

LECTURE 4 – DIGITAL ELECTRONICS



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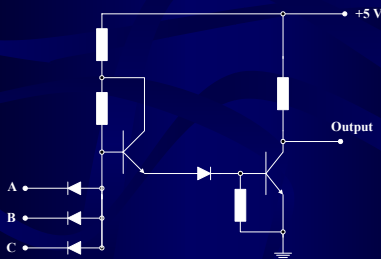
Room 153,
 Engineering Building

TTL

- In the mid – late 1960's use of resistors, diodes and transistors began to disappear
 - Discrete components phased out due to new fabrication processes
 - Processes where entire circuits could be made onto one chip
- The first to appear were small scale integration SSI
 - 1 to 10 gates or memory elements packaged as a unit
 - packaged as DIL package
- MSI medium scale integration
 - 10 to 100 gates or memory elements packaged as a unit
- LSI large scale integration
 - 100 to 10000 gates or memory elements packaged as a unit
- For MSI and LSI the popular logic family is TTL

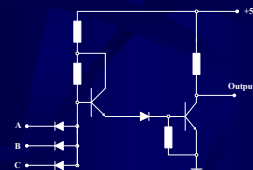
Integrated DTL NAND

- Can introduce TTL by relating it to the DTL family.
- The integrated version of the DTL NAND :



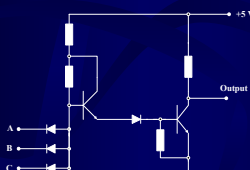
DTL

- The extra transistor adds amplification to increase fan-out
 - kept in the active region when output transistor is saturated
- Modified circuit can supply large amount of base current to the output transistor.
 - Thus output transistor can now draw a large amount of collector current before it goes out of saturation.



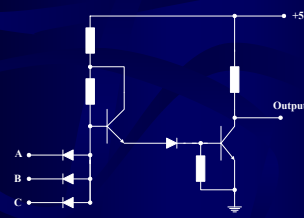
DTL

- Part of the collector current comes from the conducting diodes in the loading gates when the output transistor is saturated.
 - ⇒ an increase in allowable collector saturated current allows more loads to be connected to the output.
 - ⇒ increase fan-out capability.



DTL

- The extra diode is used to provide biasing for the output transistor
 - Avoids use of resistor
 - and need for separate negative power supply



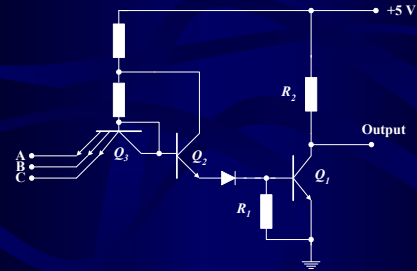
DTL → TTL

- The first change from DTL to TTL:
 - In IC's it is easier to fabricate transistors than diodes.
 - When diodes are required transistors are used
 - ⇒ Usual to use the base-emitter junction of BJT
 - ∴ base serving as the anode
 - ∴ emitter serving as the cathode
 - ∴ collector tied to the base



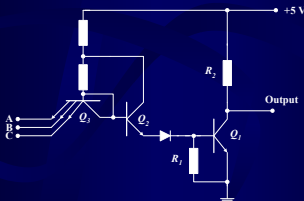
TTL: Multi-Emitter Transistor

- Note anodes of the input diodes are common
 - Thus can be realised in the form of a multiple-emitter transistor



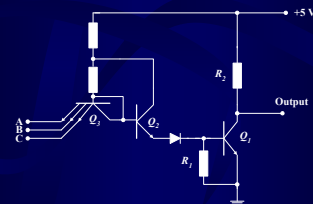
TTL : Increase Switching Speed

- The remaining changes in the evolution from DTL to TTL made to achieve increased speed.
 - When circuit is to switch from a low-output to a high-output state.
 - Q₁ must go from saturation to cut-off
 - Requires removal of charge from base of Q₁



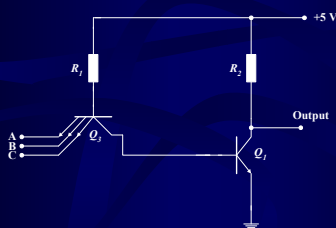
TTL : Increase Switching Speed

- Therefore this switching action is brought about by Q₂
 - Q₂ going from saturation to cut-off
- The only path for discharging the base of Q₁ through resistor R₁.
- Speed of discharge is limited by time constant of circuit.



TTL : Faster Switching

- To obtain faster switching
 - Take advantage of input diodes being realised in terms of transistors
 - change the circuit the following



- Now the charge on the base of Q₁ is removed through transistor Q₂
 - Results in a considerable reduction in the saturation delay time t_s .

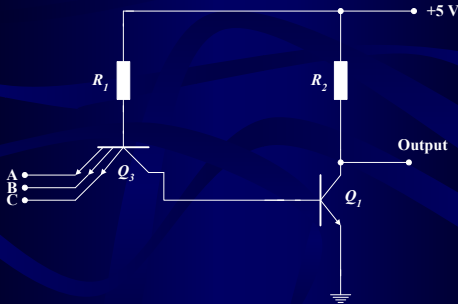
TTL : Collector Capacitance

- Another factor limiting transition speed is the collector capacitance
 - Must be charged as output voltage switches from low to high value
 - only path for charging capacitance is via the collector resistor R₂.
 - Can reduce value of R2
 - ⇒ increases charging speed

but also increases power dissipation

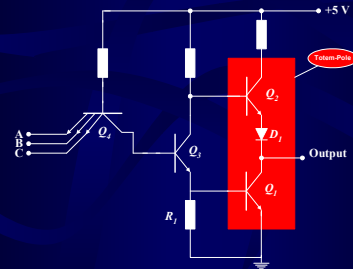
- Output circuit of this form known as **passive pull-up circuit**.
 - Output capacitance is "pulled-up" via passive element R₂.

Passive Pull up Circuit



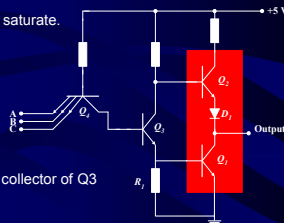
TTL : Active Pull Up Circuit

- An alternative which provides faster charging without increased power dissipation
 - the *active pull-up circuit*.



In output Low condition

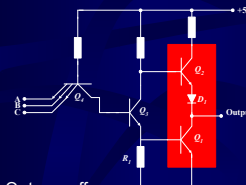
- The phase splitter transistor Q_3 is in saturation
- The saturation current through R_1 large enough to cause positive voltage drop
 - ⇒ This positive voltage causes Q_1 to saturate.
- Base of Q_2 is at 0.8 V
 - due to V_{BE} of Q_1 at 0.7 V
 - and V_{CE} of Q_3 at 0.1 V
- Because of D_1 ,
 - emitter of Q_2 is more positive than collector of Q_3
 - ⇒ Q_2 is off



D_1 in the circuit to ensure that Q_2 is cut-off when Q_1 saturated.

In output High condition

- Output High due to one of the inputs dropping low
 - ⇒ Q_3 and Q_1 go into cut-off
- However output remains momentarily low
 - as voltage across load capacitance cannot change instantaneously



- As soon as Q_3 turns off
 - ⇒ Q_2 conducts as its base is connected to V_{CC} via resistor.
- Current needed to charge load capacitance causes Q_2 to momentarily saturate
 - ⇒ output voltage rises with a time constant RC

In output High condition

- But as the Resistance R is typically :

Collector resistance of 130Ω +
resistance of the diode + saturation resistance of $Q_2 = 150\Omega$

- The value of R is \ll passive pull-up resistance used in the open collector circuit

Transition from Low to High is much faster

Changes in Capacitive load

As the capacitive load charges
⇒ the output voltage rises and current in Q_2 decreases
⇒ brings transistor into active region when in steady state condition

- Q_2 acts as an emitter follower as output terminal essentially at its emitter
 - In contrast to other transistors Q_2 is in active region
 - due to charging of capacitive loads
- ⇒ Thus the output circuit effectively acts as a two pole switch
 - switching the output between ground and the supply voltage

Metrics

- V_{OH}, V_{OL}
 $V_{CC} = +5\text{ V}$ but due to voltage drops in the output circuit
 $\Rightarrow V_{OL} = 0.2\text{ V}$ (V_{CE} of Q_2)
 $\Rightarrow V_{OH} = 3.6\text{ V}$ ($V_{CC} - (V_{BE} \text{ of } Q_2 + D_1)$)
- Speed
 - standard TTL is 3 times faster than DTL
- Fan-out
 - 8-10
- **NOTE**
 - High inputs at A, B and C will have to supply a small diode leakage current, $I_{IH} = 10\text{ }\mu\text{A}$
 - If one or more inputs are low, substantial current will flow through input terminal to ground, $I_{IL} = 1\text{ mA}$

Metrics :

- With Q_1 on
 - $\Rightarrow V_{out}$ will be a very low voltage
 - V_{OL} depends on how much collector current Q_1 conducts
- With Q_2 off
 - No current from +5 V supply through collector resistance.
 - Can only come from inputs to which gate is connected.
- Q_1 performs a current sinking action
 - called the *pull-down transistor*
- With Q_2 on
 - Q_2 supplies input current required by Q_1 of other load gates
 - Performs current sourcing actions
 - called the *pull-up transistor*

Advantages of the Totem Pole Output Stage

1. Same output could be generated without Q_2 and D_1 and connecting resistor to collector of Q_1 .

However
 $\Rightarrow Q_1$ would conduct a fairly large current in saturation state

$$\frac{+5\text{ V}}{\text{Collector Resistance}} = \frac{5}{130} \approx 40\text{mA}$$

with Q_2 in circuit
 \Rightarrow no current through collector resistance in low state
 \Rightarrow keeps power dissipation in circuit low.

Advantages of the Totem Pole Output Stage

2. In the high state
 - Q_2 acts as an emitter follower with associated low o/p impedance ($10\text{ }\Omega$)
 - Provides a short time constant for charging capacitive load on the output
 - This action, known as active pull-up provides faster switching times

Disadvantages of the Totem Pole Output Stage

1. In transition from Low – High output state
 - Q_1 turns off much faster than Q_2 turns on
 \Rightarrow few nanoseconds when **BOTH** conduct.
 - relatively high current 30 –40 mA will be drawn from supply.
 - current spike generates noise on power supply distribution line
 - if change in state is frequent
 \Rightarrow power dissipation increases.

The Standard TTL series Characteristics

1964 Texas Instruments introduced first line of standard TTL IC's.

- 54/74 series
- one of the most widely used series
- known as the 74 series (54 wider temperature range)

Many semiconductor IC manufactures now produce TTL IC's

- Fortunately all use the same numbering system
- Allowing interchanging of components

SN74	<i>Texas Instruments 74 Series</i>
DM74	<i>National Semiconductor 74 Series</i>
S74	<i>Signetics 74 Series</i>

\Rightarrow e.g. a quad 2-input NAND \Rightarrow 00 SN7400

The Standard TTL series Characteristics

- Several other TTL series have been developed since the introduction of the 74 standard series.
 - 74LS, 74S etc.
- Provide a wide choice of speed and power characteristics

NOTE

- whenever we use TTL we mean the 74 series.

The Standard TTL series Characteristics

The propagation delay of a transistor which goes into saturation.

- depends on two factors
- Saturation delay (storage time delay)
- RC time constant

By reducing resistor values

- reduces RC time constant
- decreases propagation delay

Trade-off is high power dissipation

- lower resistance draws more current from the power supply

$$\text{Speed of gate} \propto \frac{1}{\text{Propagation Delay}}$$

Low Power, 74L series

Similar as standard TTL

But all resistor values have been **increased**.

- ⇒ low power dissipation **1 mW**
- ⇒ greater propagation delay **33 nseconds**

- good for applications with low frequency, battery operated circuits
 - calculators etc.

High Speed, 74H series

Similar as standard TTL

But all resistor values have been **reduced**.

- Emitter follower has been replaced by a double emitter follower (Darlington Pair)

- ⇒ faster switching ⇒ propagation delay **6 nseconds**
- but
- ⇒ increased power dissipation **23 mW**

How to increase speed ?

Whatever is done to the value of the resistors

- Speed is ultimately limited by the time required to pull the output transistors out of saturation.
- 74, 74L and 74H series all operate with saturated switching
 - many of the transistors, when conducting will be in a saturated condition
- As has been seen this causes a saturation delay (storage delay), when switching from ON to OFF
 - limits the circuit's switching speed.

Schottky TTL, 74S series

Can this be improved ?

In Schottky TTL (STTL)

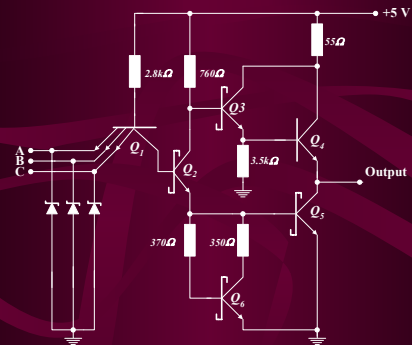
- Transistors kept out of saturation by using Schottky barrier diodes (SD)
- Formed by a junction of a metal and semiconductor
 - conventional diode with a junction of *p*-type and *n*-type semiconductor material
 - SD connected between the base and the collector
 - Do not allow the transistors to go as deeply into saturation
 - SD has a forward voltage drop of 0.4V



Schottky TTL, 74S series

- When the Collector-Base junction becomes forward biased at the on-set of saturation
 - ⇒ SD will conduct, diverting some input current away from base.
 - ⇒ this has effect of reducing the excess base current.
 - ⇒ decreases saturation (storage time) delay at turn-off
- 74S00 NAND has average propagation delay of 3 nsecs
 - twice as fast as the 74H00
 - makes the 74H series redundant nowadays

Schottky TTL, 74S series



Schottky TTL, 74S series

- Schottky Transistor used
 - 3 Schottky diodes inserted to limit negative inputs values
 - no diode in the Totem-pole output
- Circuit also uses smaller resistor values to improve switching times
- Improves the circuit average power dissipation to 20 mW

NOTE

- All transistor are Schottky Transistors.
- Q4 is not required to be a Schottky as it does not saturate but stays in active region

Schottky TTL, 74S series

- New combination of Q3 and Q6 still gives the two V_{BE} drops
 - necessary to prevent Q4 from conducting when the output is low.
 - Combination comprises a double-emitter follower (Darlington pair)
 - Provides high current gain and extremely low resistance
 - needed during the low-to high swing of the output
 - rapid output rise time when switching ON-to-OFF
- ⇒ Results in a decrease in propagation delay.

DIODES

- Diodes at input help clamp any **ringing** that may occur in the input lines
- Under transient switching conditions, signal lines appear inductive.
- this effect along with stray capacitance causes signals to oscillate or "ring".

When the output of a gate switches from high to low state

- Ringing waveforms at the input may have excursions as great as 2 - 3V (depending on line length)

DIODES

- Diodes connected to ground clamp this ringing since they conduct as soon as the negative voltage exceeds 0.4 V.
- When the negative excursion is limited, positive is also limited.
- **The success of the clamp diodes in limiting line effects has been so successful that all versions of TTL gates use them.**

The emitter resistor of Q1 form the Totem-pole NAND

- now replaced by Q6 and two resistors
- effect is to reduce turn-off current spike discussed previously

Low Power Schottky TTL, 74LS series

74 LS is a low powered version of the 74S series

- uses Schottky clamped configuration
- but with larger resistor values than 74S

Low circuit power requirements

but at the expense of increase in switching times.

- Power Dissipation 2 mW
- Propagation Delay 9.5 nseconds

This is the mainstay of the TTL family

- Found in nearly all new designs that do not require max speed.

Advanced Schottky TTL, 74AS series

- As a result of the recent development in IC design and manufacturing process
 - High speed Schottky diodes

- Power Dissipation 8 mW
- Propagation Delay 1.7 nseconds

Advanced Low-Power Schottky TTL, 74ALS series

Improvement in both power and speed.

- Power Dissipation 1.2 mW
- Propagation Delay 4 nseconds

This series has

- the lowest speed-power product of the TTL series
- very close to the lowest gate power dissipation (c.f. 74L)

This **will eventually** replace 74LS as the most widely used TTL series.

Comparison of TTL Series Characteristics

		74	74L	74H	74S	74LS	74AS	74ALS
Performance Ratings	Propagation Delay (nSec)	9	33	6	3	9.5	1.7	4
	Power Dissipation (mW)	10	1	23	20	2	8	1.2
	Speed Power (pJ)	90	33	138	60	19	13.6	4.8
	Max Clock rate (MHz)	35	3	50	125	45	200	70
	Fan-out (same series)	10	20	10	20	20	40	20
Voltage Parameters	V _{OH} (min)	2.4	2.4	2.4	2.7	2.7	2.5	2.5
	V _{OL} (max)	0.4	0.4	0.4	0.5	0.5	0.5	0.4
	V _{IH} (min)	2.0	2.0	2.0	2.0	2.0	2.0	2.0
	V _{IL} (max)	0.8	0.7	0.8	0.8	0.8	0.8	0.8

All of the performance ratings are for a NAND gate in each series.

Speed Power (picoJoules)

- low value required.

The Maximum Clock Rate :

- specified as the maximum frequency that can be used to toggle a J-K flip-flop.
- Gives a measure of the frequency range over which each series can be operated.

Differences in TTL family are not in Logic Levels

- But in internal construction of the basic NAND gate.