

# LECTURE 11 – DIGITAL ELECTRONICS



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## CMOS

- Complementary MOS (CMOS) Inverter analysis makes use of both NMOS and PMOS transistors in the same logic gate.
- All static parameters of CMOS inverters are superior to those of NMOS inverters
- Price paid for these substantial improvements
  - Increased process complexity to provide isolated transistors of both polarity types.

## CMOS

- CMOS most widely used digital circuit technology in comparison to other logic families.
  - lowest power dissipation
  - highest packing density
- ⇒ Virtually all modern microprocessors are manufactured in CMOS and older version are now reprocessed in CMOS technology.
- Advantage of having both transistors in the same logic gate comes from the value of  $V_{GS}$  needed to enable the Drain-Source current channel.

## CMOS

- |         |                      |                                      |
|---------|----------------------|--------------------------------------|
| logic 1 | (Positive $V_{GS}$ ) | turns on an NMOS<br>turns off a PMOS |
| logic 0 |                      | turns off an NMOS<br>turns on a PMOS |
- ⇒ Thus for the output high and low states both devices are **never** on simultaneously
- NMOS acts as the output transistor and the PMOS acts as the load transistor.
    - ⇒ output pull-up and pull-down paths never conflict during operation of the CMOS inverter

## CMOS

PMOS operation summarised as :

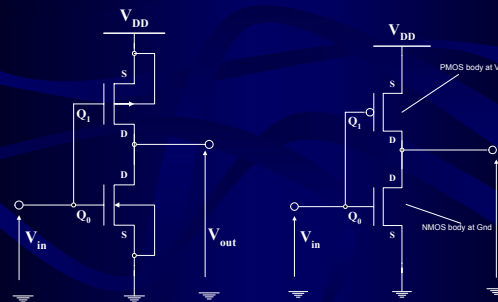
⇒ Cutoff:  $V_{SG,P} \leq -V_{T,P}$

⇒ Linear:  $V_{SG,P} \geq -V_{T,P}$  and  $V_{SD,P} \leq V_{SG,P} + V_{T,P}$

⇒ Saturation:  $V_{SG,P} \geq -V_{T,P}$  and  $V_{SD,P} \geq V_{SG,P} + V_{T,P}$

## CMOS

- By connecting the complementary transistors as below, can create an inverter.



## CMOS

- NMOS enhancement-mode transistor is the lower  $Q_0$
- PMOS enhancement-mode transistor is the upper  $Q_1$

Gates are connected together  $\Rightarrow V_{in} = V_{GS,N} = V_{DD} - V_{SG,P}$

Drains are connected together  $\Rightarrow V_{out} = V_{DS,N} = V_{DD} - V_{SD,P}$

### NOTE :

- Other transistor can be considered the load for the other.
- Consider  $Q_0$  as the load for  $Q_1$ , in the PMOS inverter configuration is just as correct as considering  $Q_1$  as the load on the NMOS inverting transistor.  
 $\Rightarrow$  the operation of  $Q_0$  and  $Q_1$  "complement" each other.

## VTC for the CMOS Inverter: $V_{OH}$

- In determining the VTC for a CMOS inverter, consider  $V_{in}=0$

NMOS  $\Rightarrow V_{GS,N} = V_{in} = 0 < V_{T,N} \Rightarrow Q_0$  cut-off  
 $I_{D,N} = 0$

PMOS  $\Rightarrow V_{SG,P} = V_{DD} - V_{in} = V_{DD} > -V_{T,P}$

and  $V_{SD} < V_{DD} + V_{T,P}$  PMOS in linear mode

## $V_{OH}$

However  $I_{D,P} = I_{D,N} \Rightarrow$  Drain Current of PMOS = 0

$$\Rightarrow I_{D,P} = 0 = \beta_P \left[ (V_{SG,P} + V_{T,P}) - \frac{V_{SD,P}}{2} \right] V_{SD,P}$$

which gives the solution that  $V_{SD,P} = 0$

However, since

$$\begin{aligned} V_{SD,P} &= V_{DD} - V_{out} \\ \Rightarrow V_{out} &= V_{DD} = V_{OH} \end{aligned}$$

## $V_{OL}$

For  $V_{in} = V_{OH} = V_{DD} \Rightarrow Q_0$  (NMOS) in the linear region  
 $Q_1$  (PMOS) cut-off

$V_{DS,N}$  found by solving  $I_{D,N}(Lin) = I_{D,P}(off) = 0$

$$I_{D,N} = 0 = \beta_N \left[ (V_{GS,N} + V_{T,N}) - \frac{V_{DS,N}}{2} \right] V_{DS,N}$$

which gives the solution that  $V_{DS,N} = 0$

$\Rightarrow$  the output for  $V_{in} = V_{DD}$  is  $V_{OL} = V_{DS,N} = 0$

## $V_{OL}$

- Unlike the NMOS inverter configurations, the output of a CMOS inverter does reduce all the way to 0V.

- Since output can range from 0 volts to VDD

$\Rightarrow$  output is said to "rail-to-rail"

## Calculation of VTC

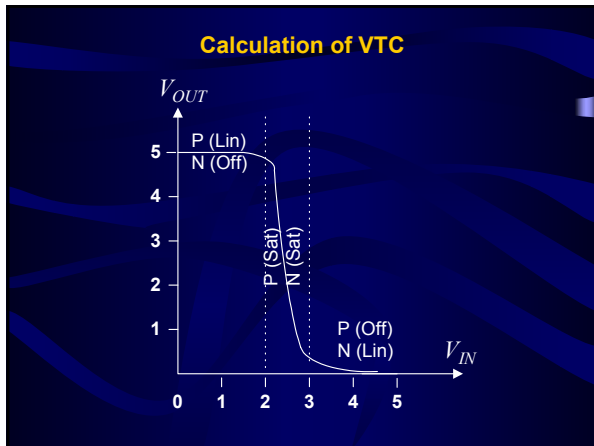
- Find critical points,  $V_{OH}$ ,  $V_{OL}$ ,  $V_{IL}$  and  $V_{IH}$ .

$V_{IL} \Rightarrow$  NMOS operation in saturation region  
 PMOS operates in linear mode

- Equate currents to obtain  $V_{IL}$  and corresponding output voltage.

$V_{IH} \Rightarrow$  NMOS operation in linear region  
 PMOS operates in saturation mode

- Equate currents to obtain  $V_{IH}$  and corresponding output voltage.



### Static Power Dissipation of CMOS

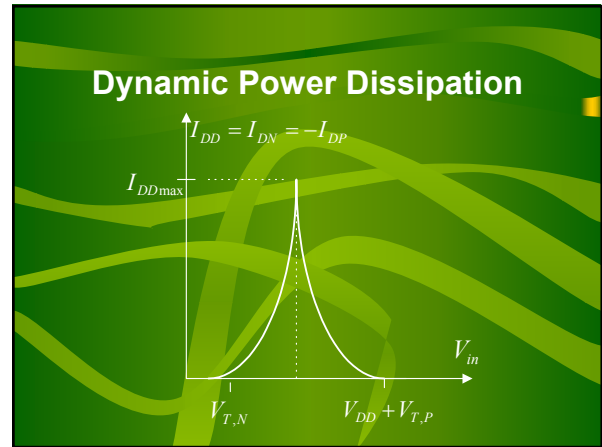
For  $V_{OH} \Rightarrow$  NMOS in cut-off  $\Rightarrow I_{D,N} = 0$   
 For  $V_{OL} \Rightarrow$  PMOS in cut-off  $\Rightarrow -I_{D,P} = 0$   
 Since  $I_{DD} = I_{D,N} = -I_{D,P}$   
 $\Rightarrow$  current supplied by  $V_{DD}$  for both output states is zero.  
 i.e.  $I_{DD}(OH) = I_{D,N}(OFF) = 0$   
 $I_{DD}(OL) = I_{D,P}(OFF) = 0$   
 $\Rightarrow$  no static power dissipation for CMOS inverter

$$P_{DD}(avg) = \frac{I_{DD}(OH) + I_{DD}(OL)}{2} \cdot V_{DD}$$

$$P_{DD}(avg) = \frac{0 + 0}{2} \cdot V_{DD} = 0$$

### Dynamic Power Dissipation

- Both MOS devices are active in the transition state, between  $V_{IL} < V_{IN} < V_{IH}$
- Power is dissipated during the switching between the two outputs states of the CMOS inverter



### Dynamic Power Dissipation

- Dynamic power dissipated =  $P_{DD}(dyn) = C_T \nu V_{DD}^2$

$C_T$  = total load capacitance  
 $\nu$  = frequency of switching

- The extremely low power dissipation of CMOS has made possible applications that could never exist when using any of the NMOS families.

### Example

- Determine the Power Dissipation in a CMOS inverter with  $V_{DD} = 5V$ , operating at 25MHz and a load capacitance of 0.05pF.

Answer: 31.25  $\mu W$

## Design of Symmetric CMOS Inverters

- A valuable aspect of CMOS is that a **symmetric** VTC is **easily obtainable**.
- One reason for designing with a symmetric VTC is to obtain a symmetric transient response.

## Design of Symmetric CMOS Inverters

- To achieve a symmetric VTC
  - The threshold voltages are made equal in magnitude by using ion implantation.

$$\beta_N = \beta_P$$

$$k'_N \frac{W_N}{L_N} = k'_P \frac{W_P}{L_P}$$

## Design of Symmetric CMOS Inverters

- The process transconductance parameters for each N- an P-Channel MOS device are :

$$k'_N = \mu_N C_{OX}$$

$$k'_P = \mu_P C_{OX}$$

$$\mu_N C_{OX} \frac{W_N}{L_N} = \mu_P C_{OX} \frac{W_P}{L_P}$$

- usually the gate oxide layers of the NMOS and PMOS devices are grown simultaneously
  - ⇒ have the same thickness  $t_{OX}$

## Design of Symmetric CMOS Inverters

and since  $C_{OX} = \frac{\epsilon_{OX}}{t_{OX}}$

⇒ simultaneous growth of the oxide layers results in the same  $C_{OX}$

$$\mu_N \frac{W_N}{L_N} = \mu_P \frac{W_P}{L_P}$$

## Design of Symmetric CMOS Inverters

- Typically for the surface of Silicon the electron and hole mobilities are approximately:

$$\mu_N(Si) = 580 \text{ cm}^2/\text{V}\cdot\text{Sec}$$

$$\mu_P(Si) = 230 \text{ cm}^2/\text{V}\cdot\text{Sec}$$

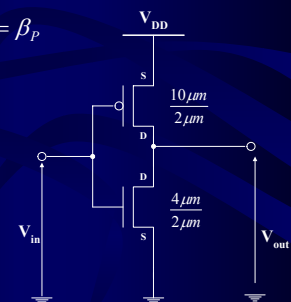
$$\Rightarrow 580 \frac{W_N}{L_N} = 230 \frac{W_P}{L_P}$$

$$\Rightarrow \frac{W_P}{L_P} = 2.5 \frac{W_N}{L_N}$$

## Design of Symmetric CMOS Inverters

- Hence to have  $\beta_N = \beta_P$

⇒



## CMOS Noise Margins

$$\begin{aligned} V_{OL} &= 0V & V_{OH} &= V_{DD} \\ V_{IL} &= 30\% V_{DD} & V_{IH} &= 70\% V_{DD} \\ V_{NH} &= V_{OH} - V_{IH} & V_{NL} &= V_{IL} - V_{OL} \\ &= V_{DD} - 70\%V_{DD} & &= 70\%V_{DD} - 0 \\ &= 30\%V_{DD} & &= 30\%V_{DD} \end{aligned}$$

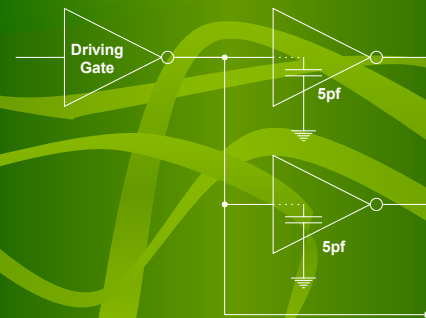
## CMOS Noise Margins

- Noise margins are same in both states and depend on  $V_{DD}$ .
  - At  $V_{DD} = 5V \Rightarrow$  noise margins are both **1.5V**
  - Substantially better than TTL and ECL
- This makes CMOS attractive for applications that are exposed to high noise environments.
- Noise margins can be made even wider by using a higher value of  $V_{DD}$ .
  - improvement obtained at the expense of a higher drain on the power because of the higher supply voltage.

## CMOS Fan-Out

- Fan-out analysis of BJT logic circuits
  - considers the maximum current a driving logic gate can source or sink from the inputs of connected load gates during either output low or high states.
- Fan-out limitation of a CMOS gate involves how much capacitance can be driven with the gate still having acceptable propagation delays
  - Each CMOS input typically presents a 5pf load to ground.
  - $\Rightarrow$  CMOS output has to charge and discharge the parallel combination of all the input capacitances
  - $\Rightarrow$  **Thus output switching time will be increased in proportion to the number of load being driven.**

## Fan-Out



## Example

- The driving inverter gate above, may have a typical  $t_{PLH}$  of 25 nseconds if driving no loads  
But when driving 20 loads  $\Rightarrow 25nsec + 20(3) = 85nsec$
- CMOS fan-out depends on the permissible maximum propagation delay.
  - $\Rightarrow$  for low freq. operation  $\leq 1MHz \Rightarrow$  fan-out limited to 50
  - $\Rightarrow$  for high freq. operation  $\Rightarrow$  fan-out  $< 50$

## CMOS Series Characteristics

- Several different series in CMOS family of IC's.
- 4000
  - 4000 series, which was introduced by RCA (14000 by Motorola) was the first CMOS series.
    - Original series was the 4000A series.
    - Improved version is the 400B series, with higher output current capabilities.
  - 4000 series is widely used despite emergence of new CMOS series. The 4000 series has been manufactured much longer and has many functions not yet available in the newer series.

## CMOS Series Characteristics

### 74C series

- This CMOS series is compatible pin-for-pin and function-by-function for the TTL devices having the same number.
  - Not all functions that are available in TTL are available in CMOS series.
  - Can replace some TTL circuits by an equivalent CMOS design.

## CMOS Series Characteristics

### 74HC (High Speed) series

- Main improvement is a 10-fold increase in switching speed
  - Comparable to 74LS TTL series

### 74HCT series

- Also high speed CMOS series. The major difference between this and the 74HC series is that it is designed to be voltage-compatible with TTL devices.

⇒ it can be directly driven by a TTL output.

⇒ this is this is not the case with other CMOS devices.

## Comparison of Digital IC Families

Performance Ratings	74HC	4000B	74	74S	74LS	74AS	74ALS	ECL
Power Dissipation/gate (mW)								
Static	2.5x10 <sup>3</sup>	1x10 <sup>3</sup>	10	20	2	8	1.2	40
@ 10MHz	0.17	0.1	10	20	2	8	1.2	40
Propagation Delay (nSec)	9	50	9	3	9.5	1.7	4	1
Speed Power Product @ 10MHz	1.4	5	90	10	19	13.6	4.8	40
Max Clock rate (MHz)	40	12	35	12.5	45	200	70	300
Voltage Parameters								
Worst Case Noise Margin	0.9	1.5	0.4	0.3	0.3	0.3	0.4	0.25

All of the performance ratings are for a 1k/10p gate in each series.

## Particular Notes on CMOS

- All CMOS inputs on a package (eg. Multi-gate chip) must be connected to a fixed voltage 0v or  $V_{DD}$  or another input.
  - Applies to even to inputs of extra unused logic gates on a chip.
    - An unconnected CMOS input is susceptible to noise and static charges that could easily bias both the P and N channel devices in the conductive state
      - ⇒ increased power dissipation & overheating.

## Particular Notes on CMOS

- High input resistance of CMOS inputs makes them especially prone to static-charge build-up that can produce voltages large enough to break down the dielectric insulation between the FET's gate and channel.
  - Most of newer CMOS devices have protected Zener diodes on each input.
  - Diodes are designed to turn-on and limit the size of the input voltage to well below any damage value.
  - While diodes usually function fine, sometimes they do not turn on quickly enough to prevent the IC from being damaged
    - good practice to use special handling