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Fundamentals of Electronic Circuit Design

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BY
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1- *Atomic Structure*

1.1 The nature of the Atom

The atom consist of nucleus of positive charge that contains nearly all the mass of atom. It surrounding by negative charges called electrons.

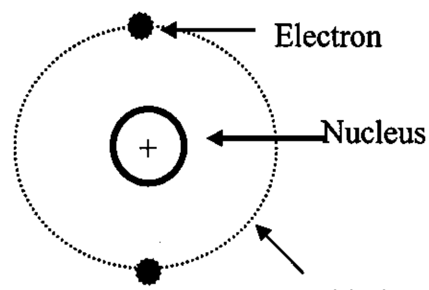


Fig. (1) Atom structure

The charge of proton (inside the nucleus) equal to the electrons charge. The fource of the the attraction between electron and proton follows by **Columb's Law.**

1.2 Bohr Atom

The hydrogen contain one electron in his orbital call (Bohr Atom). Three are two attractive Force

F_P : Potential Force

F_K : Kinetic Force.

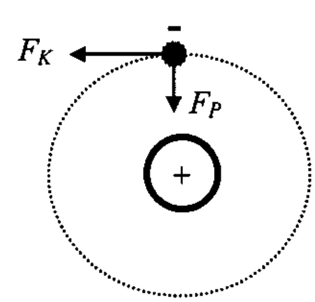


Fig. (2) Bohr Atom (H^+)

$$F_P = \frac{e^2}{4\pi\varepsilon_0 r^2} \qquad (1)$$

$$F_K = \frac{m\,v^2}{r} \qquad (2)$$

where

e : electron Charge = 1.602 *10^{-19} C

m : electron mass = 9.11*10^{-31} Kg

ε_0 : permittivity of air = 8.859 *10^{-12} F/m

v : velocity of electron (m/sec)

r : rides of electron (m)

The condition for equilibrium the two force is equal, that lead to

$$\frac{e^2}{2\pi\varepsilon_0 r^2} = \frac{m\,v^2}{r}$$

$$v^2 = \frac{e^2}{4\pi\varepsilon_0 m\,r} \qquad (3)$$

The stationary state is determined by the condition, the angular momentum of electron in this state be integral multiple of $h/(2\pi)$ as

$$m\,v\,r = \frac{n\,h}{2\pi} \qquad (4)$$

where

h : Plank'c constant = 6.626 * 10^{-34} J.sec

n : orbital number

$$v = \frac{n\,h}{2\pi\;m\,r} \qquad (5)$$

by using Eq. (3) by Eq. (5) the result is

$$r = \frac{h^2\varepsilon_0}{\pi\;m\,e^2}n^2 \qquad (6)$$

by using Eq.(3) with Eq.(6) the *r* by

$$v = \frac{e^2}{2\, h\, \varepsilon_0} \frac{1}{n} \qquad (7)$$

1.3Atomic Energy

There are two type of energy at the atom.

i- **Potential Energy** E_P of electron at distance r from the nucleus

$$E_P = \frac{-e^2}{4\pi\varepsilon_0 r} \qquad (8$$

ii. **Kinetic Energy** E_K for the electron moving around the nucles

$$E_K = \frac{m\, v^2}{2} \qquad (9)$$

therefore the total Energy are

$$E_T = E_P + E_K$$

$$E_T = E_P + E_K = \frac{m\, v^2}{2} + \frac{-e^2}{4\pi\varepsilon_0 r}$$

$$E_T = \frac{-e^4}{8\pi\varepsilon_0 r} = \frac{-m\, e^4}{8h^2 \varepsilon_0^{\ 2}} \frac{1}{n^2} \ (Joule) \qquad (10)$$

$$E_T(ev) = E_T(J)/e$$

$$E_T = \frac{-13.6}{n^2} \ (ev)$$

ev : the electron volt unit.

1.4 Atomic Energy Levels

For the integral values of n in Eq.(4) horizontal line is drown. A convenient pictorial representation is called as (Energy- level diagram) Fig.(3).

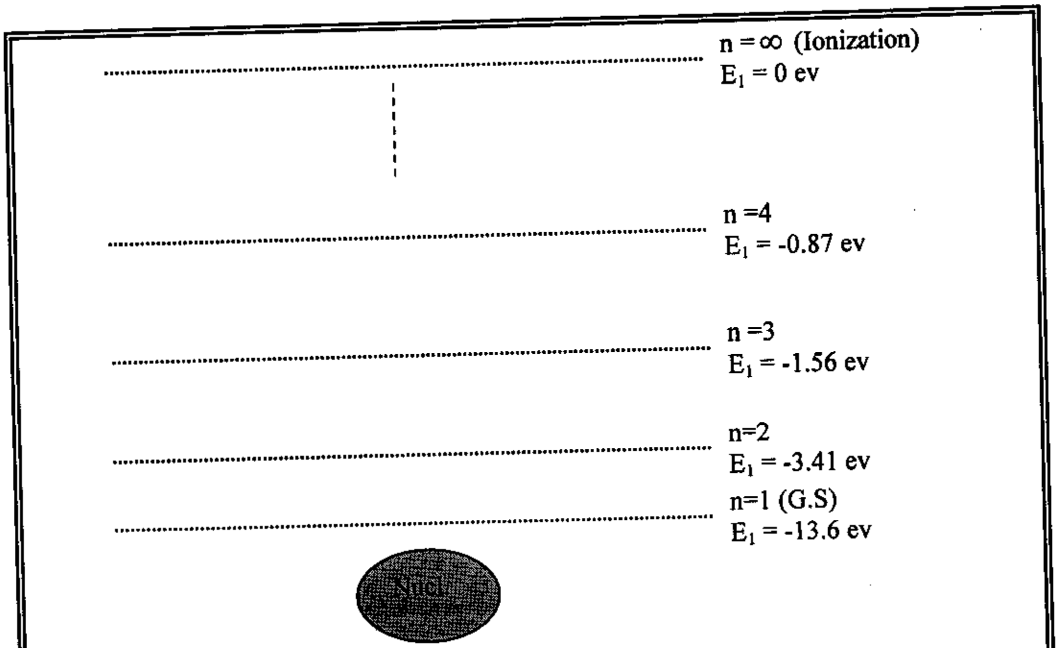


Fig. (3) The Energy levels of Bohr atom (H^+)

The Ionization level is the level of number $n = \infty$. The atom by ionize is absorbed energy equal to the level energy.

1.5 *Photo Affective*

The electron in ground state (G.S) absorbed an light (Photon) then transfer to upper state this case call photon absorbsion, if the photon transfer from upper state to lower state radiate photons this case call photon emission. The photon Energy E_{Ph} calculated by

$$E_{Ph} = h\,f = \frac{h\,C}{\lambda} \qquad (11)$$

where

f: Photon frequency (Hz)

λ : Photon wavelength (m)

C : light velocity = $3*10^8$ (m/sec)

Hint: Angistrom (A^0) = 10^{-10} m

a- *Absorbsion*

The electron in Lower level absorbed photon energy and transfer into upper level with low energy Fig.(4). The energy of final orbital can calculate his energy by

$$E_f = E_i + hf \quad (12)$$

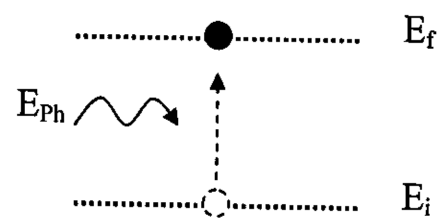


Fig.(4) Absorbsion

If photon Energy greater or equal to the Energy level then the electron transfer to level n= Inf., the atom in this case call Ionize and this phenomena call **Photo ionization** see Fig. (5).

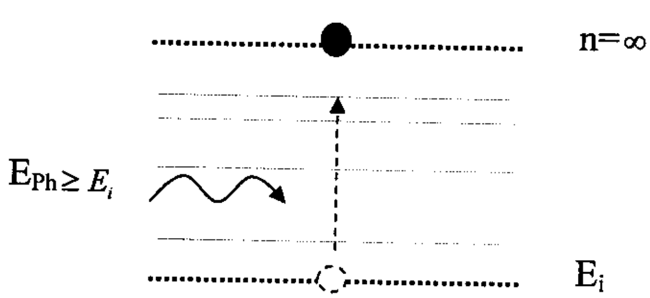


Fig.(5) Photo Ionization

b- *Emission*

An atom has been raised from the ground state to an exited level by electron bombardment. The excited electron returning to it's previous state. In this case the electron loss the amount of energy as photon (Light), this phenomena called (Emission). The Photon energy calculated by

$$E_{Ph} = hf = E_f - E_i \quad (13)$$

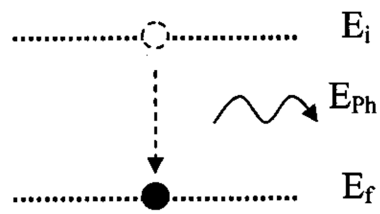


Fig.(6) Emission

The return electron gives more probability for emission photon frequency, the number of photons frequency depend on the number of initial orbital. For example, if the initial orbital n_i then

Probability of Emission Photon =(n-1)!

> **Example:** the electron in fourth level, calculate probability of emission photon?
>
> Sol./ Fourth orbital n=5
>
> Prob. =5! =1*2*3*4*5 =120 case

1.6 Another Atoms

In hydrogen atom (Bohr atoms) atomic number Z=1. Therefore, for another atoms of atomic number Z the eqs.(6, 7, and 10) by

$$r = \frac{h^2 \varepsilon_0}{\pi\, m\, e^2 Z^2} n^2 \qquad\qquad v = \frac{e^2}{2\, h\, \varepsilon_0} \frac{Z}{n}$$

$$E_T \frac{-m\, e^4}{8h^2\varepsilon_0^{\,2}} \frac{Z^2}{n^2} \ (Joule)$$

$$E_T = \frac{-13.6}{n^2}\ Z^2 (ev)$$

Sheet (1)

Q_1) In Bohr atom an electron in G.S absorbed Photon of wavelength 1026A^0 find

i- The final orbital number

ii- If the electron on new orbital transfer to orbital (n=5) what happen.

iii- Emitting Photon wavelength if the electron return to second orbital.

iv- Calculate the rides and velocity of electron in second level

Q_2) Electron in third orbital calculate the photon wavelength that absorbed to ionized the atom.

Q_3) Prove that emission photon wavelength in Bohr atom calculated from

$$\lambda = \frac{12400}{E_f - E_i} \qquad A^0$$

Q_4) Drive the total electron energy in Bohr atom

Q_5) Prove

i. $E_T = \frac{E_P}{2}$

ii. $E_T = -E_K$

Q_6) Calculate minimum Emitted Light wavelength to convert Bohr atom from Ionized to atom.

2 *Material Types*

There are three type of material :

i. **Insulator** is very poor conducting material the energy gap between valance band and conduction band very high.

ii. **Conductor** is excellent conducting material the energy gap between valance band and conduction band very small.

iii. **Semiconductor** is subtended material between conductor and Insolate material, the energy gap between valance band and conduction band small, for that the semiconductor is transfer case between conducted and insolated material.

Energy Band, its know as group of orbital have the same performance. There are two type of Bands, **Valance Band (V.B)** and **Conduction Band (C.B).** The electron in C.B call free electrons, this electrons cause conducing in material. As shown Fig.().

Energy Gap (E.G), it's the region separates between valence band and conduction band. The energy gap is

$$E_g = E_C - E_V \qquad .... (14)$$

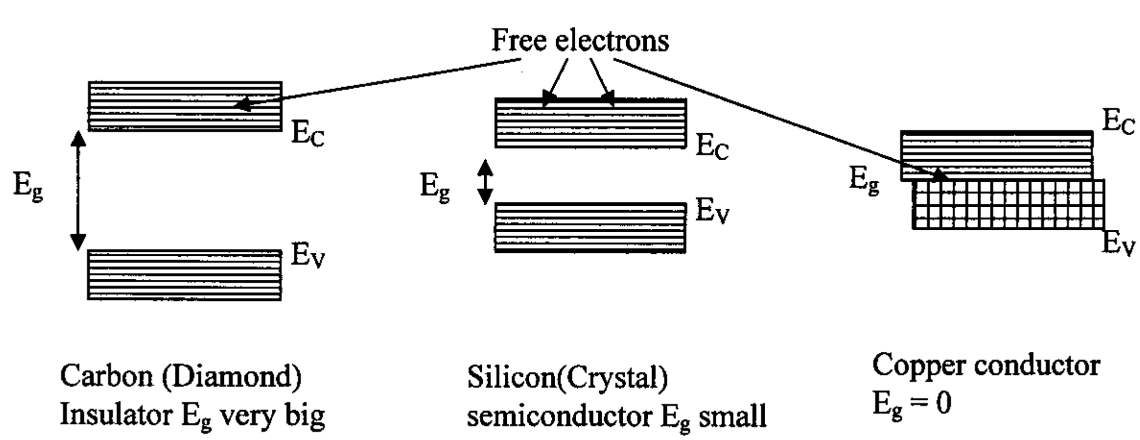


Fig. (7) material Type and Energy levels.

2.1 Interstice Semiconductor

The covalent bonding process in Silicon (Si) is illustrated in Fig.(8)

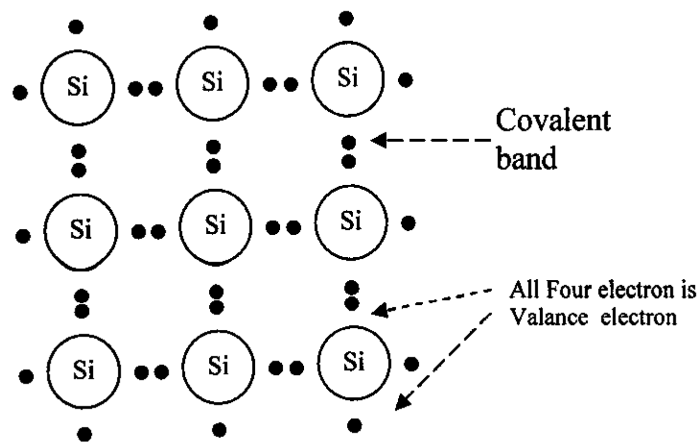


Fig. (8) Silicon Structure

Structures from by atoms bounded together covalently are called **Crystal Structures.** This semiconductor crystal call Interstice semiconductor. All the valence electron are tightly bound to the parent atom and to other atoms by *Covalent bounds*.

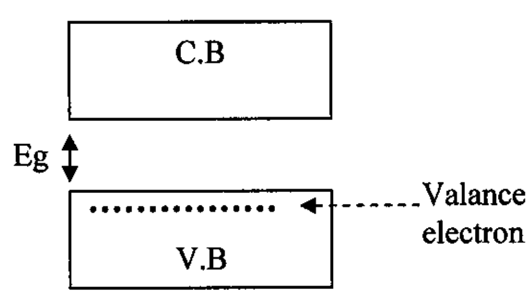


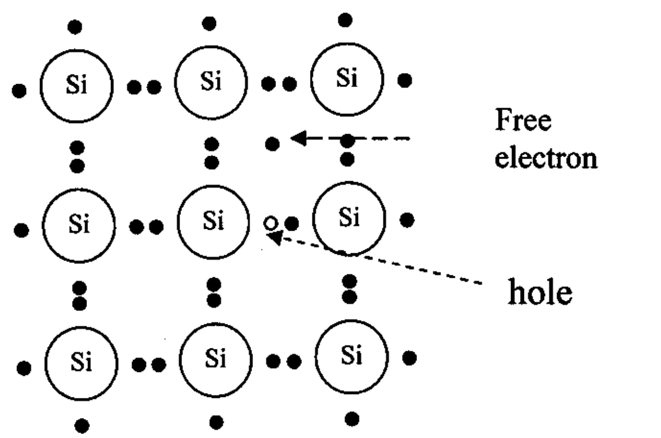
Fig. (9) Energy band diagram of Int. Si

1.6.1 Affect of Temperature

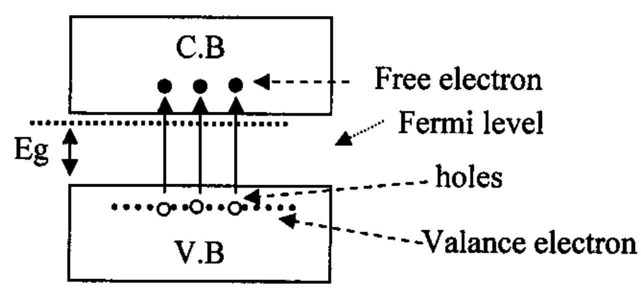
After hear energy has been applied a covalent bound broken the one of the valance electrons as a result of heat energy. The liberation of this valence electron left a vacancy in the covalent structure. This vacancy is call a ***hole***, the number of free electron (n) is equal to total number of hole (p). the (n_i) the total carrier density in interstice semiconductor calculated by

$$n_i^2 = n \times p \qquad .... (15)$$

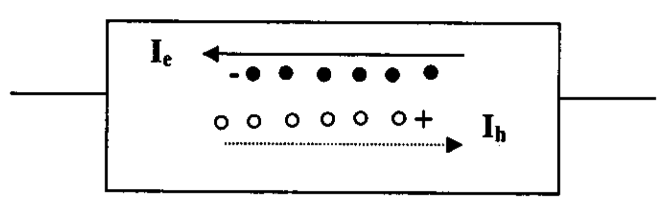
- ***Electron-hole pairs*** : the hole is created by an electron breaking a covalent bond a valence electron from a neighboring atoms can easily fill hole by free electron, for that electrons and holes moving in different side as shown in Fig.(10).



a- Silicon Structure



b- Energy band diagram of Int. Si



c- pair of Interstice Semiconductor.

Fig. (10) Effect of Temperature.

2.2 Fermi level

It can be proved that in an interstice semiconductor the Fermi level E_F lies in the middle of the energy gap between C.B and V.B. as shown in Fig.(10). The probability of find energy level is

$$P(E)=\frac{1}{1+e^{[(E-E_F)/KT_K]}} \qquad \text{.... (16)}$$

where

K : Poltizman Constant = $1.23*10^{-23}$

T_K : Temperature in Kelvin, $T_K=T^0+273$

T^0 : Temperature in degree.

Example/ Fermi Deric probability of level above of Fermi level by 0.3 ev is **1%** find Temperature in Degree.

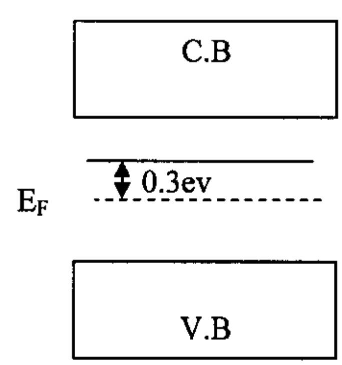
Sol.

$P(E) = 0.01$

$E\text{-}E_F = 0.3$ ev

$$P(E)=\frac{1}{1+e^{[(E-E_F)/KT_K]}}$$

$E\text{-}E_F\,(J) = 0.3(ev)*1.602*10^{-19} = 0.4806*10^{-19}$ J



$$0.01=\frac{1}{1+e^{[(0.4806*10^{-19})/1.23*10^{-23}T_K]}}$$

$$\frac{(0.4806*10^{-19})}{1.23*10^{-23}T_K}=\ln((1/0.01)-1)$$

$$T_K=\frac{(0.4806*10^{-19})}{1.23*10^{-23}*\ln(999)}$$

$T_K = 565K$

$T^0 = T_K\text{-}275 = 290^0$

2.2 Extrinsic Semiconductor

The interstice semiconductor has been doped by extremely small amounts of Three or Five electron material, this semiconductor call extrinsic.

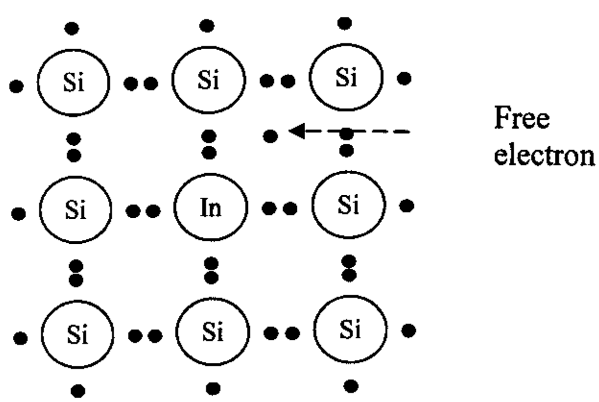
There are two type of doping

i- Pentavalent atoms have **Five** valance electron.

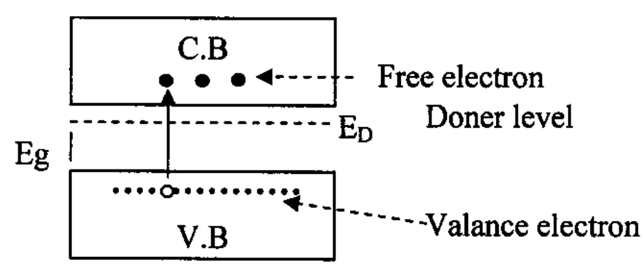
ii- Trivalent atoms have **Three** valance electron.

2.2.1 N-type Semiconductor

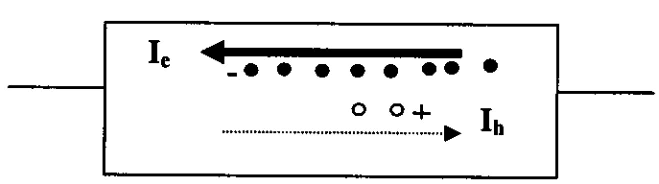
If the doping by Five velance electron materal, the number of electron increasing, that increase total number of carrier, the electrons call **majority carrier** (n_n). The hole result from electron-hole pair, it is **minority carrier** (P_n) Fig.(10-a). when doner impurities (electrons) has been add to a semiconductor allowable energy level below the conduction bound (E_D Doner Energy level), this case reduce the energy gap as shown in Fig.(10b). The main current generated from majority carrier (electron), when the hole generate minority carrier as shown in Fig. (10-c).



a- N-type Semi.



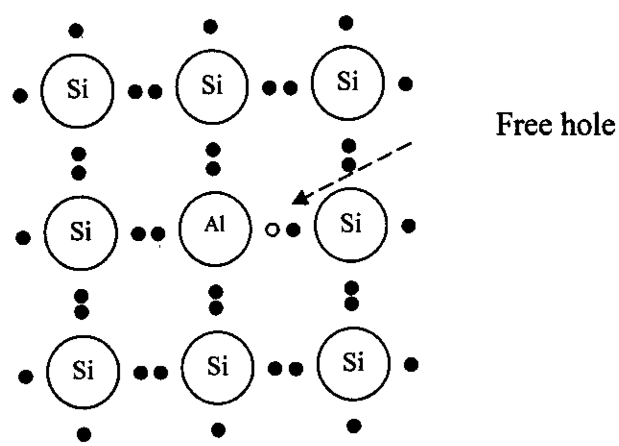
b- Energy band diagram of N-type



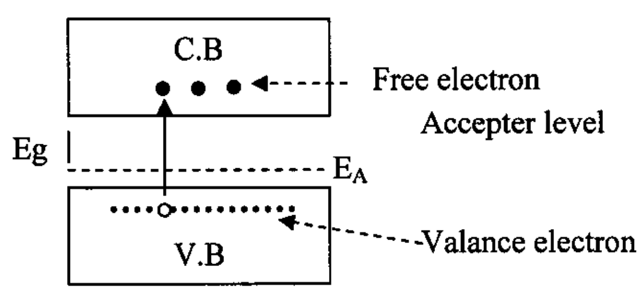
c- Pair of N-type Semiconductor (majority carrier electron).

2.2.2 P-type Semiconductor

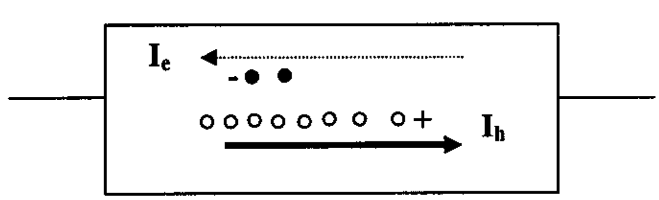
If the doping by Three valance electron material, the number of hole increasing, that increase total number of carrier. The holes call **majority carrier** (p_p). The electrons result from electron-hole pair, it is **minority carrier** (n_p) Fig.(11-a). when Accepter impurities (holes) has been add to a semiconductor allowable energy level below the conduction bound (E_A Accepter Energy level), this case reduce the energy gap as shown in Fig.(11-b). The main current generated from majority carrier (holes), when the electrons generate minority carrier as shown in Fig. (11-c).



a- P-type Semi.



b- Energy band diagram of P-type



c- Pair of P-type semiconductor (majority carrier hole).

Fig. (12) P-type Semiconductor.

2. 3 Charge Density in semiconductor

- Interstice Semiconductor

The number of electron is equal to the number of hole

$n = p$ and $n_i = n\,p$ .... (17)

- N- type Extrinsic Semiconductor

Let N_D the concentration of doner atoms,

The total number of electron (majority carrier)

$$N_D + n$$

$$n_n = N_D + n$$
$$N_D >> n \qquad \text{.... (18)}$$
$$n_n = N_D$$

the number of holes p_n (minority carrier) calculated by

$$p_n = \frac{n_i^2}{N_D} \qquad \text{.... (19)}$$

- P- type Extrinsic Semiconductor

Let N_A the concentration of Accepter atoms,

The total number of holes (majority carrier)

$$N_A + p$$

$$P_p = N_A + p$$
$$N_A >> p \qquad \text{.... (20)}$$
$$P_p = N_A$$

the number of holes n_p (minority carrier)calculated by

$$n_p = \frac{n_i^2}{N_A} \qquad \text{.... (21)}$$

2.4 Conductivity in Semiconductor

-Interstice Semiconductor

The current in semiconductor is

$$I = I_e + I_h \qquad \text{.... (22)}$$

where

I_e: current of electron (A).

I_h: current of hole (A).

The current density (*J*) is

$$J = \frac{I}{A} \qquad \text{.... (23)}$$

where

A: area cross section (m^2).

By using ohm low the current density is

$$J = \sigma\ E = \left(e\ n\ \mu_e + e\ p\ \mu_h\right)E \qquad \text{.... (24)}$$

where

σ : conductivity of material ($(\Omega.m)^{-1}$).

E: electrical filed intensity (V/m).

The total current density is

μ_e : Mobility of electrons (m^2/v.sec).

μ_h : Mobility of holes (m^2/v.sec).

from the Eq. (2.11) the conductivity calculated from

$$\sigma = \left(e\ n\ \mu_e + e\ p\ \mu_h\right) \qquad \text{.... (25)}$$

- N- type Extrinsic Semiconductor

$$\sigma_N = \left(e\ n_n\ \mu_e + e\ p_n\ \mu_h\right) \qquad \text{.... (26)}$$

because

n_n>> p_n then conductivity of hole will be neglected

then the conductivity of N – type be

$$\sigma_N = e\ N_D\ \mu_e \qquad .... (27)$$

- *P- type Extrinsic Semiconductor*

$$\sigma_p = (e\ n_p\ \mu_e + e\ p_p\ \mu_h) \qquad .... (28)$$

because

p_p>> n_p then conductivity of hole will be neglected

then the conductivity of P – type be

$$\sigma_p = e\ N_A\ \mu_h \qquad .... (29)$$

2.3.4 Semiconductor Resistance

The resistively of material is defined as

$$\rho = \frac{1}{\sigma} \qquad .... (30)$$

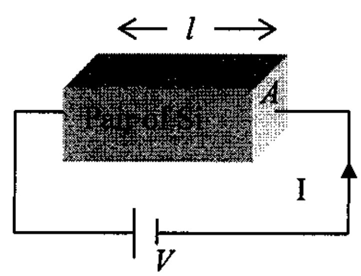


Fig.(13) Pair of Si

The applied voltage V across the pair of semiconductor is equal to

$$V = El \qquad .... (31)$$

where

E: The electrical filed intensity (v/m)

l : Pair material length (m).

The ohm's low defined the resistance of material (R) by

$$J = \sigma\ E \qquad .... (32)$$

From Eqs. (2.10), (2.18), and (2.19) the resistance by

$$\frac{I}{A}=\frac{1}{\rho}V\,l$$
$$\frac{V}{I}=\rho\frac{l}{A}=R \quad (\Omega) \qquad \ldots.. \quad (33)$$

By using Eq. (2.20) the resistance of semiconductor interstice, N-type, and P-type, respectively, defined as

$$R=\frac{l}{\sigma\;A}\quad(\Omega)\qquad R_N=\frac{l}{\sigma_N\;A}\quad(\Omega)\qquad R_P=\frac{l}{\sigma_P\;A}\quad(\Omega)\quad \ldots.\,(34)$$

Example : A specimen of pure Germanium at **300K** has density of charge carrier of **$2.5*10^{14}$ m^{-3}**. Its doped with donor impurity atoms at the rate of one impurity atom for every **10^6** atoms of Germanium. All impurity atoms may be supposed to be ionized. The density of Germanium atoms **$4.2*10^{28}$ atoms/m^{-3}** if mobility of electron and hole is **0.36 m^2/(v.sec)** and **0.18 m^2/(v.sec)**, respectively. Find 1- minority and majority carrier

2- Conductivity and resistively

Sol.

T=300K

$n_i = 2.5*10^{14}\ m^{-3}$

$N_D = 4.2*10^{28}/10^6 = 4.2*10^{22}\ m^{-3}$ *(majority)*

$p_n = n_i^2/N_D = (2.5*10^{14})^2/4.2*10^{22} = 1.4*10^6\ m^{-3}$ *(minority)*

N-type

$$\sigma_N=\left(e\;n_n\;\mu_e+e\;p_n\;\mu_h\right)=e\left(N_D\;\mu_e+p_n\;\mu_h\right)$$
$$\sigma_N=1.602\times10^{-19}(4.2\times10^{22}*0.36+1.4\times10^{6}*0.18)$$
$$\sigma_N=2.42\times10^{3}\qquad(\Omega.m)^{-1}$$
$$\rho_n=\frac{1}{\sigma_N}=\frac{1}{2.42\times10^{3}}=0.41\times10^{-3}\qquad\Omega.m$$

Sheet-2

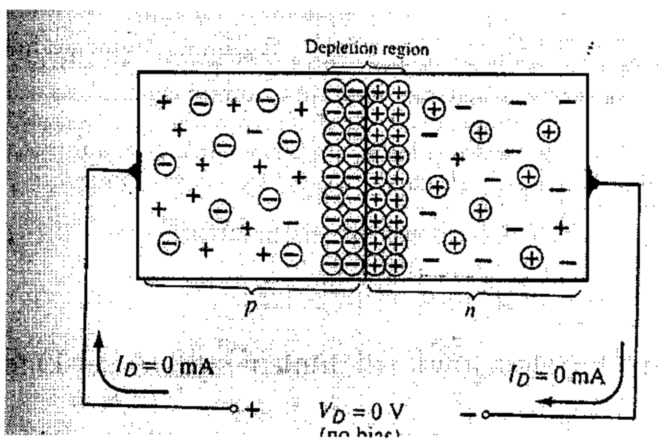
Q_1/ Fermi Deric probability of level below of Fermi level by 0.3 ev is **90%** find Temperature in Degree.

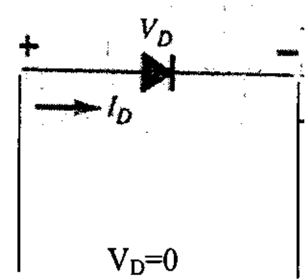
Q_2/ Fermi Deric probability of level below of Fermi level by a ev is **90%** at Temperature 500 K find (a).

Q_3/ Cylindrical tube of germanium of length **1mm** and radius **0.05 mm** have carrier density $4.5*10^{-3}$ cm^{-3}. It's doped with acceptor impurity atoms at rate of one atom to every 10^6 atoms of germanium. The total number of atoms per unit volumes $5.31*10^{32}$ atoms.m^{-3}.

3. P-N Junction (Diode)

The semiconductor diode is formed by simple bringing of N-type and P-type semiconductor, this materials together generate diode as shown in Fig.(14). At the instant the two material are joined the electrons and holes. The region of the junction will combine resulting in alack of carriers, this region call **Depletion region**.





Diode Symbol

Fig.(14) P-N junction diode.

3.1 Diode Bias

If the external potential of **V volt** is applied across the P-N junction this will bias the diode. There are two type of diode bias

- Reverse Bias

The Positive terminal to N-type and the negative terminal to P-type as shown in Fig.(15-a). The depletion region have been winded, that result to over come the region from the majority carrier more and more carrier. The current that exists under reverse-bias condition call **Reverse Saturation Current (I_S).**

- Forward Bias

The Positive terminal to P-type and the negative terminal to N-type as shown in Fig.(15-b). The application of **F.B** potential V_D. The electrons in N-type and hole in P-type will be recombine with the ions near the boundary region and reduce the width of depletion region. The Diode current pass $\mathbf{I_D}$ calculated by

$$I_D = I_S\left(\exp^{(eV_D/\ KT)} - 1\right)$$

Where

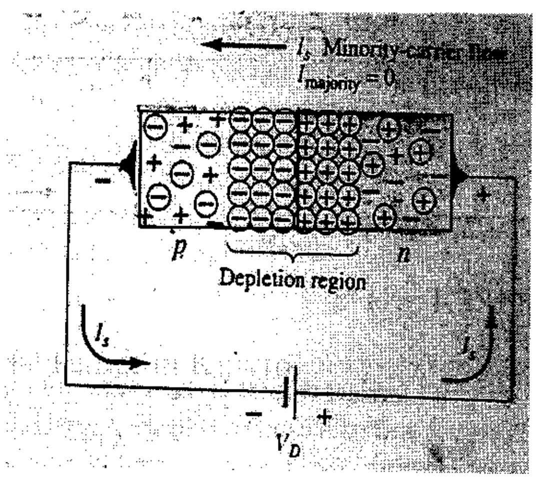
V_D : applied voltage:

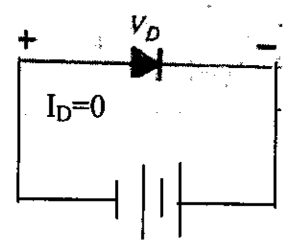
K: Boltizman Constant. ($K=1.38*10^{-23}$ J/k)

T: Temp. in Kelvin.

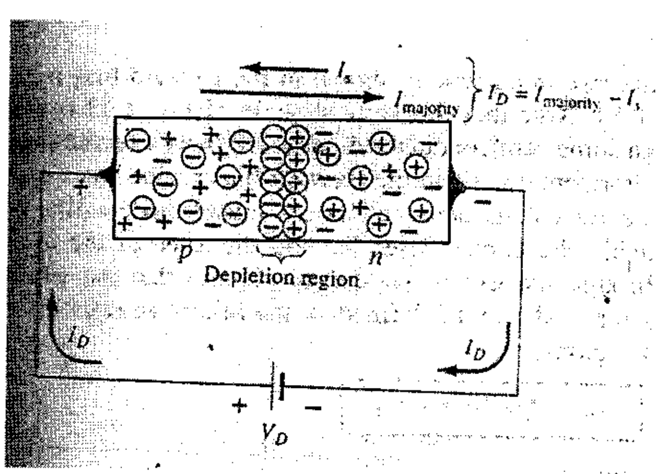
T^0: temp. in degree.

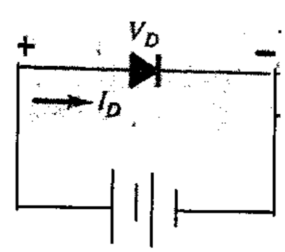
$$T=T^0+273$$





(a)



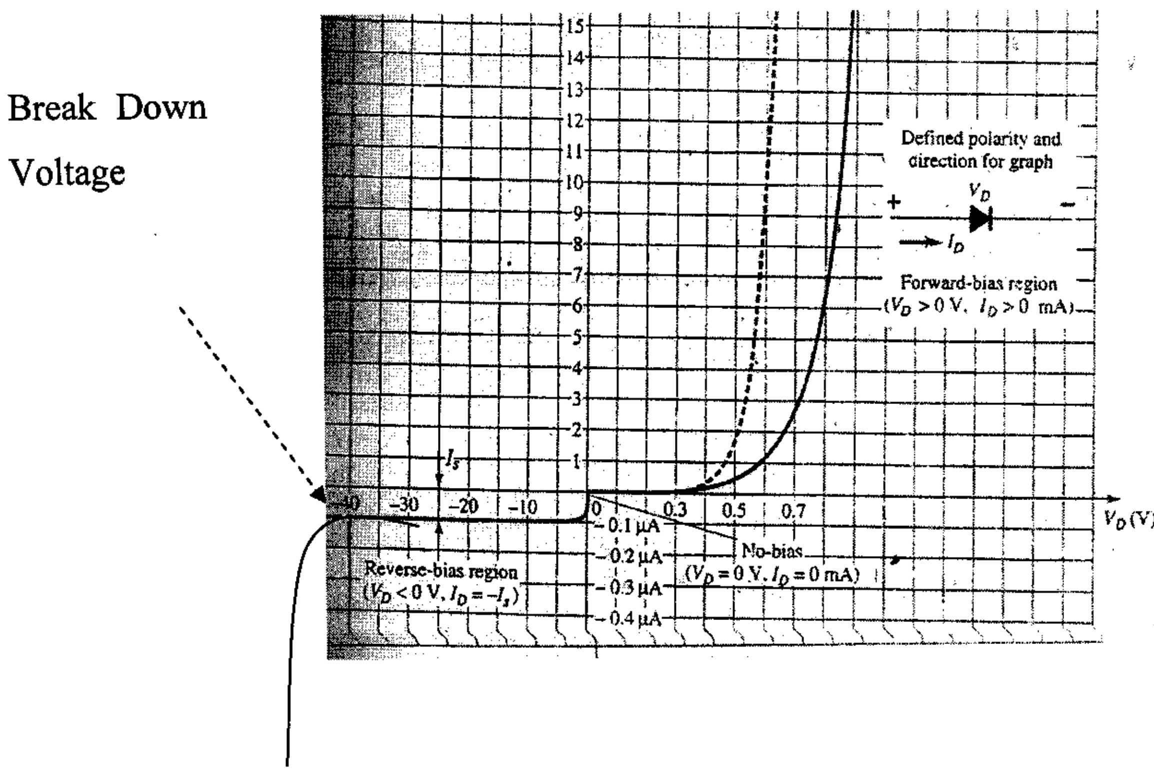


(b)

Fig.(15) a. Reverse bias diode b. Forward bias diode

3.2 *V- I Diode Characteristics*

The relation ship between applied voltage $\mathbf{V_D}$ and diode current $\mathbf{I_D}$ can draw as



The **break down region** is the reverse voltage that destroyed the reverse bias depletion region and flow current in **R.B.**

3.3 Diode Resistance

The diode resistance can calculated depend on type of applied voltage

- D.C Diode Resistance

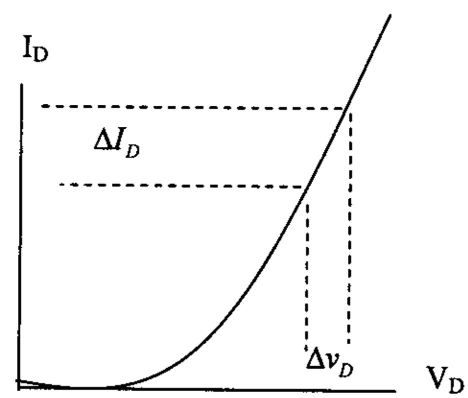
$$R_D = \frac{V_D}{I_D}$$

Where

R_D: diode resistance in DC.

- a.c Diode Resistance

The derivative of a function at point is equal to the slope of the tangent line draw at the point



$$I_D = I_S(\exp^{(eV_D/KT)} - 1)$$

$$\frac{dI_D}{dV_D} = I_S(\exp^{(eV_D/KT)} \cdot \frac{e}{KT})$$

$$\frac{dI_D}{dV_D} = \frac{e}{KT}(I_D + I_S)$$

$$\frac{dI_D}{dV_D} \approx \frac{e}{KT} I_D$$

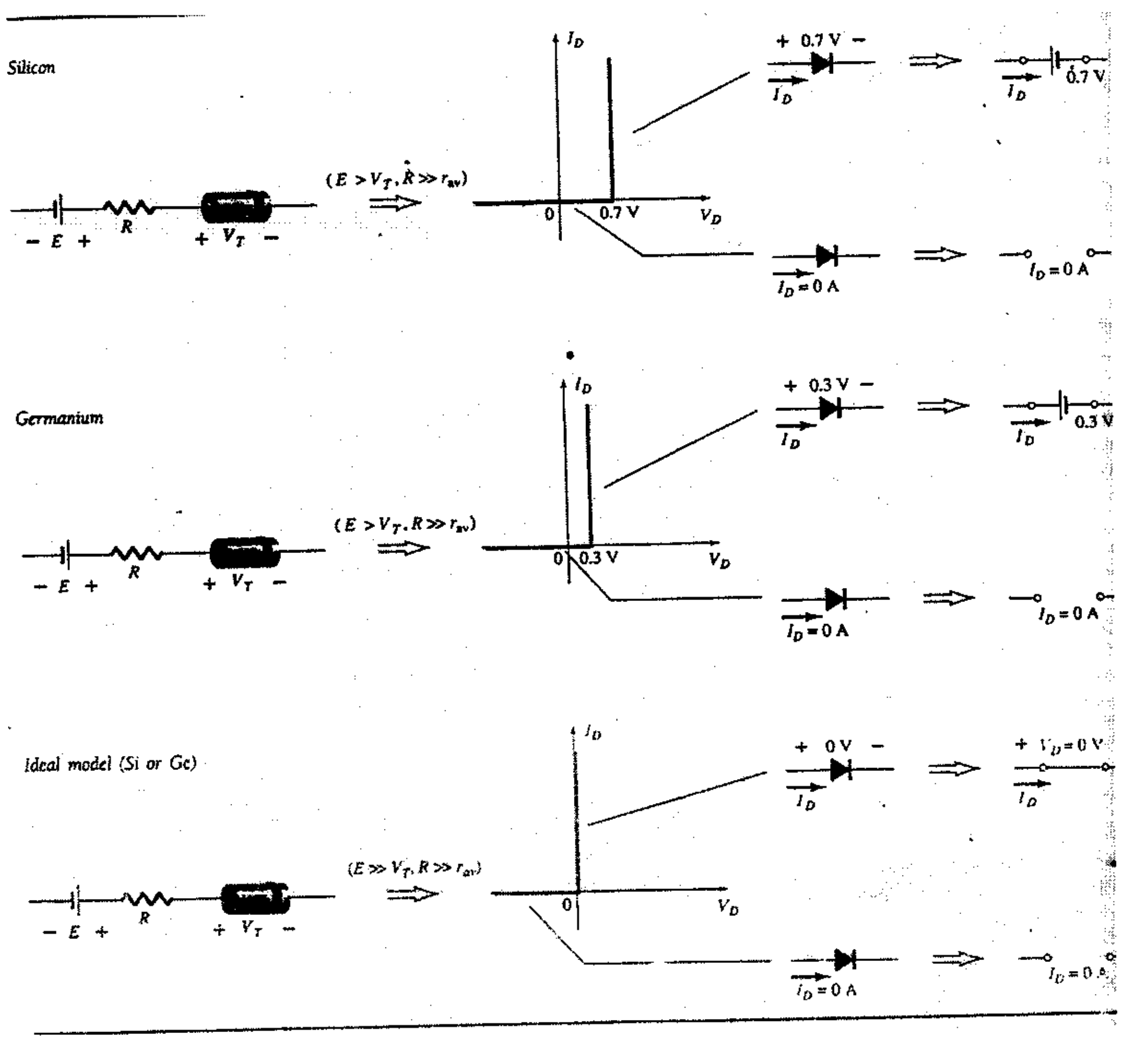
$$at\ room\ temp.\ T = 300k$$

$$r_D = \frac{dV_D}{dI_D}$$

$$r_D = \frac{0.026}{I_D}\ \Omega$$

3.4 Diode Equivalent cct.

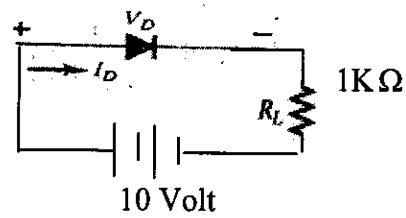
Diode equivalent cct. in both F.B and R.B shown in Fig.(14)



Power dissipated in diode is

$$P_{Diode} = V_{D.}\ I_D$$

Example/ For the cct. shown below find V_D, I_D and R_D at room temp.



Sol/

From the cct.

$V - V_D - I_D R_L = 0$

$V_D - 1000\, I_D = 10$ (1)

$$I_D = I_S\left(\exp^{(eV_D/\ KT)} - 1\right)$$

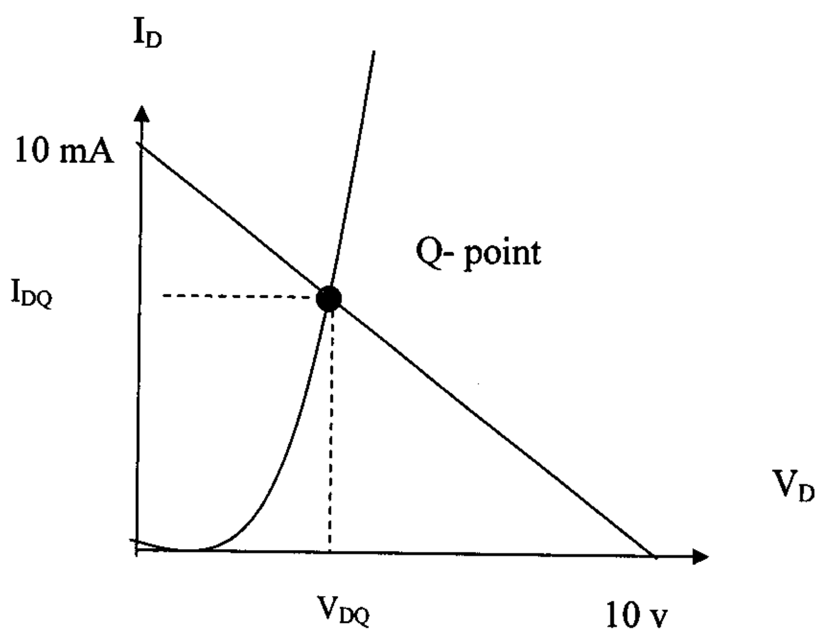
$$I_D = 0.1*10^{-6}\left(\exp^{(V_D/11600)} - 1\right) \qquad (2)$$

Using draw to find I_D and V_D

Equation (1)

$V_D=0$ $I_D=10$ mA

$I_D=0$ $V_D=10$ V



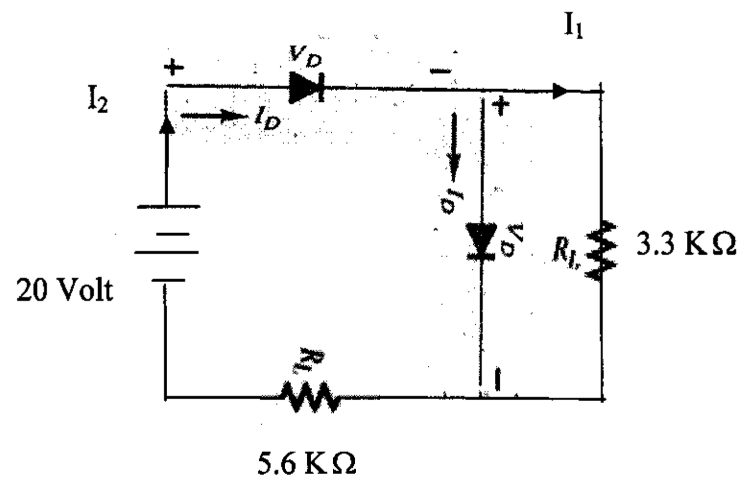
$V_{DQ}=0.8$ volt

$V_{DQ}=9.8$ mA

$R_D=0.8/9.8*10^{-3}= 81.6\ \Omega$

Example/ Determined the currents I_1, I_2, and I_{D2} for the cct. shown below.

Both diode silicon diode



Sol/

D_1 : F.B D_2 : F.B

$V_{D1} = V_{D1} = 0.7$ volt

$I_1 = V_{D2}/R$

$I_1 = 0.7/3.3*10^3 = 0.212$ mA

By using K.V.L (the close loop is)

$I_2 = (20 - V_{D1} - V_{D2})/ R_L$

$I_2 = (20-0.7-0.7)/ 5.6*10^3 = 3.32$ mA

$I_{D2} = I_2 - I_1$

$I_{D2} = 3.108$ mA

4 Diode a.c Applications

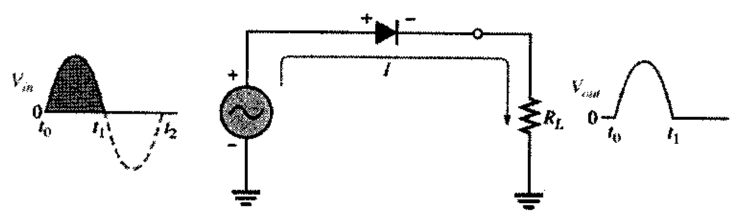
4.1 Rectifier

A rectifier is an electrical circuit used to convert AC voltage into DC voltage. The are two type of rectifiers

- Half-Wave Rectifier (HWR)

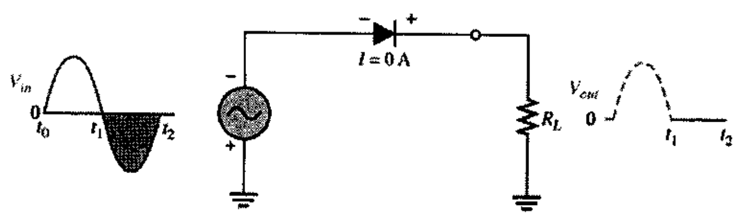
The process of **half-wave rectification** is illustrated below

Positive Cycle



(a) During the positive alternation of the 60 Hz input voltage, the output voltage looks like the positive half of the input voltage. The current ,..... .. through ground back to the source.

Negative Cycle



(b) During the negative alternation of the input voltage, the current is 0, so the output voltage is also 0.

(c) half-wave output voltage for three input cycles

Fig.(16) HWR cct.

- When sinusoidal input (V_{in}) goes positive, diode is Forward Biased (F.B), thus conducts current. The output voltage keeps the shape of the input voltage.
- When V_{in} becomes negative (second half of cycle), diode is reverse biased (RB). There is no current the voltage across resistor R_L is 0V.
- Net result is a pulsating dc voltage with same frequency as input.

Average value (DC value) of HWR signal is

$$V_{DC} = \frac{V_{p(out)}}{\pi}$$

Where

$V_{p(out)}$: the peak output voltage.

The root mean square value (RMS value) of HWR signal is

$$V_{rms} = \frac{V_{p(out)}}{2}$$

For non-ideal diode (Silicon diode) the peak output voltage decreases by 0.7 V as

$$V_{p(out)} = V_{p(in)} - 0.7$$

Peak Inverse Voltage (PIV)

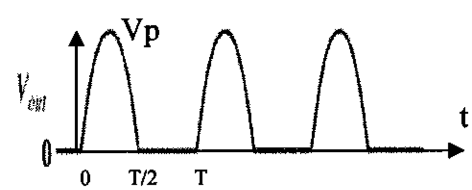
Diode must be able to withstand this amount of repetitive reverse voltage, PIV calculate from diode in reverse bias. PIV in HWR is equal to peak value of the input voltage.

$$PIV = V_{p(in)}$$

Example/ prove for HWR

i. $V_{DC} = \frac{V_{p(out)}}{\pi}$ **ii.** $V_{rms} = \frac{V_{p(out)}}{2}$

Sol.



$$V_{out}(t) = \begin{cases} Vp\sin(\omega t) & 0 \le t < T/2 \\ 0 & T/2 \le t \le T \end{cases}$$

$$V_{DC} = \frac{1}{T}\int_{-T/2}^{T/2} V_{out}(t)\ dt$$

$$V_{DC} = \frac{1}{T}\left[\int_{0}^{T/2} Vp\sin(\omega t)\ dt + \int_{T/2}^{T} 0\ dt\right]$$

$$V_{DC} = \frac{Vp}{T}\left[\int_{0}^{T/2} \sin(\omega t)\ dt\right]$$

$$V_{DC} = \frac{-Vp}{T\omega}\cos(\omega t)\ \Big|_{0}^{T/2}$$

$$V_{DC} = \frac{-Vp}{T\omega}[\cos(\omega T/2) - \cos(0)]$$

$$V_{DC} = \frac{2Vp}{T\frac{2\pi}{T}}$$

$$V_{DC} = \frac{Vp}{\pi}$$

II.

$$V_{rms} = \sqrt{\frac{1}{T}\int_{-T/2}^{T/2}(V_{out}(t))^2\,dt}$$

$$V_{rms} = \sqrt{\frac{1}{T}\left[\int_{0}^{T/2}(Vp\sin(\omega t))^2\,dt + \int_{T/2}^{T}0\,dt\right]}$$

$$V_{rms} = \sqrt{\frac{Vp^2}{T}\left[\int_{0}^{T/2}\frac{1-\cos(\omega t)}{2}\,dt\right]}$$

$$V_{rms} = \sqrt{\frac{Vp^2}{T}\left[\frac{1}{2}t - \frac{1}{4\omega}\sin(\omega t)\right]_0^{T/2}}$$

$$V_{rms} = \sqrt{\frac{Vp^2}{T}\frac{T}{4}} = \frac{Vp}{2}$$

- Full-Wave Rectifier (FWR)

The Full-Wave Rectifiers are the most commonly used ones for dc power supplies. The FWR exactly the same as the half-wave, but allows unidirectional current through the load during the entire sinusoidal cycle (as opposed to only half the cycle in the half-wave) as shown in Fig.(17). The frequency of the output is twice that of the input. There are two main types of full wave rectifiers:

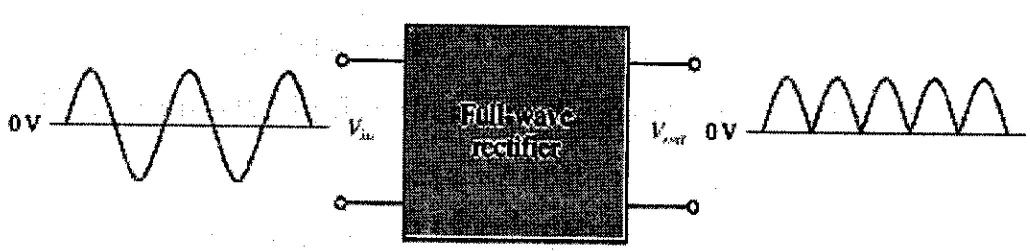
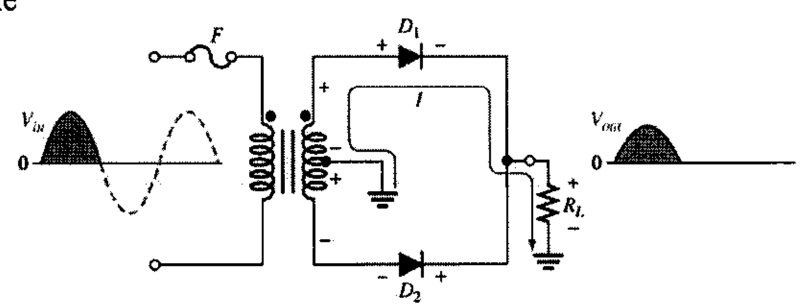


Fig. (17) The FWR output wave form

1- Center-tapped transform FWR

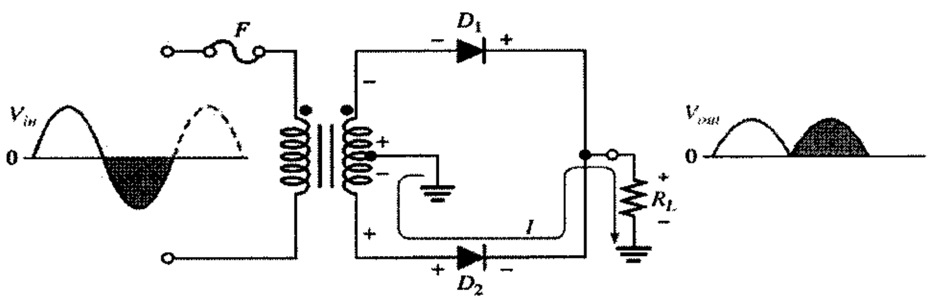
Two diodes connected to the secondary of a center-tapped transformer as shown in Fig.(18). Half of V_{in} shows up between the center tap and each secondary $V_{p(sec)}$. At any point in time, only one of the diodes is forward biased. This allows for continuous conduction through load.

- Positive Cycle
D_1 : F.B
D_2 : R.B



(a) During positive half-cycles, D_1 is forward-biased and D_2 is reverse-biased.

- Negative Cycle
D_1 : R.B
D_2 : F.B



(b) During negative half-cycles, D_2 is forward-biased and D_1 is reverse-biased.

Fig. (18) The FWR center tab transformer circuit.

Average value (DC value) of FWR center-tap signal is

$$V_{DC} = \frac{2\ V_{p(out)}}{\pi}$$

The root mean square value (RMS value) of HWR signal is

$$V_{rms} = \frac{V_{p(out)}}{\sqrt{2}}$$

For non-ideal diode (Silicon diode) the peak output voltage decreases by 0.7 V as

$$V_{p(out)} = V_{p(sec)} - 0.7$$

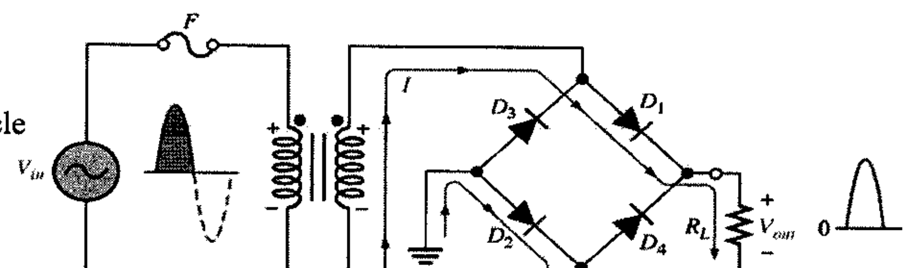
PIV in FWR center-tab is

$$PIV = V_{p(sec)} + V_{p(out)} = 2\ V_{p(sec)} + 0.7$$

2- Bridge full-wave rectifier.

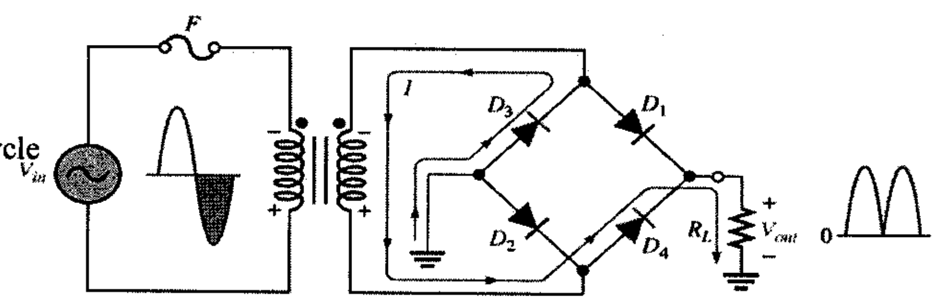
Four diodes connected to transform as shown in Fig.(19). Every two diode work together in one cycle of signal.

- Positive Cycle
D_1, D_3 : F.B
D_2, D_4 : R.B



(a) During positive half-cycle of the input, D_1 and D_2 are forward-biased and conduct current. D_3 and D_4 are reverse-biased.

- Negative Cycle
D_1, D_3 : R.B
D_2, D_4 : F.B



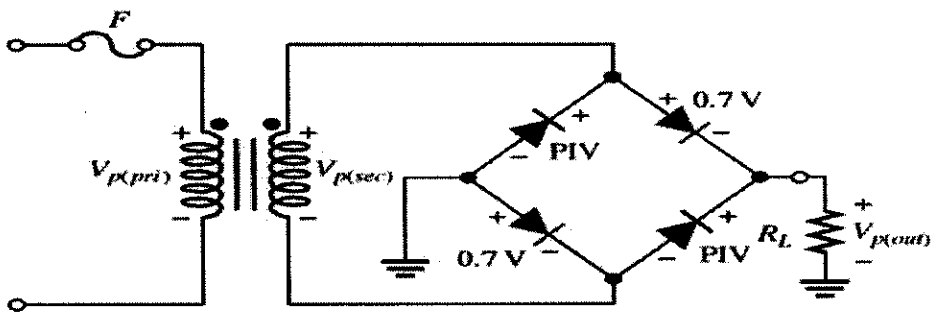
(b) During negative half-cycle of the input, D_3 and D_4 are forward-biased and conduct current. D_1 and D_2 are reverse-biased.

Fig.(19) The FWR cct. (**Bridge rectifier**)

When the input cycle is positive, diodes D_1 and D_2 are forward biased. When the input cycle is negative, diodes D_3 and D_4 are the ones conducing. The output voltage becomes:

$$V_{p(out)} = V_{p(sec)} - 1.4\ V$$

The reason we'd rather use a full bridge rectifier than a center-tap, is that the PIV is a lot smaller as shown in Fig.(20)



(b) For the practical diode model (forward-biased diodes D_1 and D_2 are shown in blue). PIV = $V_{p(out)}$ + 0.7 V

Fig.(20) The FWR Bridge rectifier, calculate PIV.

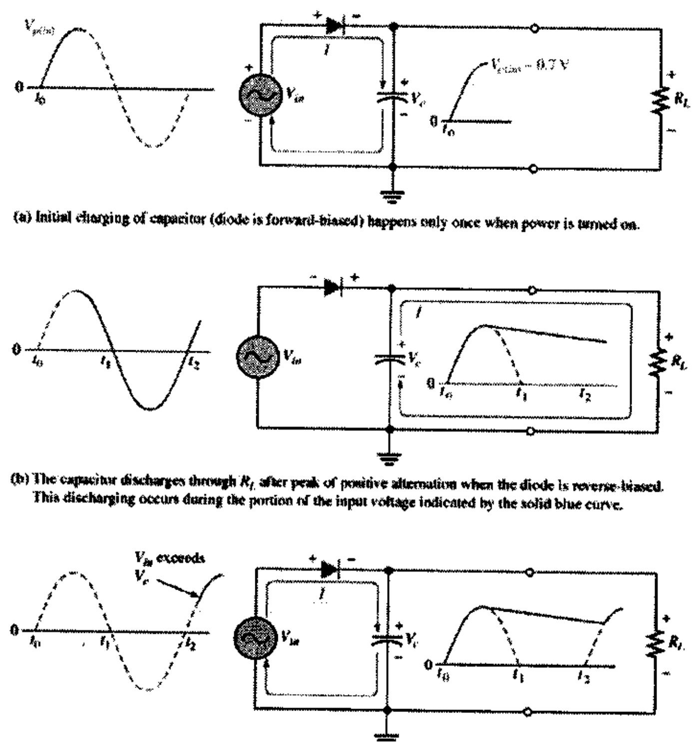
$$PIV = V_{p(out)} + 0.7$$

Q/ prove for FWR

i. $V_{DC} = \frac{2V_{p(out)}}{\pi}$ **ii.** $V_{rms} = \frac{V_{p(out)}}{\sqrt{2}}$

3- Rectifier with filters (regulators)

The output of the rectifier is a pulsating dc wave. To generate a constant dc output use filter out the oscillations from the pulsating dc wave. The diode capacitor combination is the first type of regulator as shown in Fig. (21). A capacitor-input filter will charge and discharge such that it fills in the “gaps” between each peak. This reduces variations of voltage. This voltage variation is called ripple voltage V_r. The advantage of a full-wave rectifier over a half-wave is shown in Fig. (22) . The capacitor can more effectively reduce the ripple when the time between peaks is shorter.



(a) Initial charging of capacitor (diode is forward-biased) happens only once when power is turned on.

(b) The capacitor discharges through R_L after peak of positive alternation when the diode is reverse-biased. This discharging occurs during the portion of the input voltage indicated by the solid blue curve.

(c) The capacitor charges back to peak of input when the diode becomes forward-biased. This charging occurs during the portion of the input voltage indicated by the solid blue curve.

Fig.(21) the affect of capacitor at HWR output signal

The ripple voltage and ripple factor calculated by

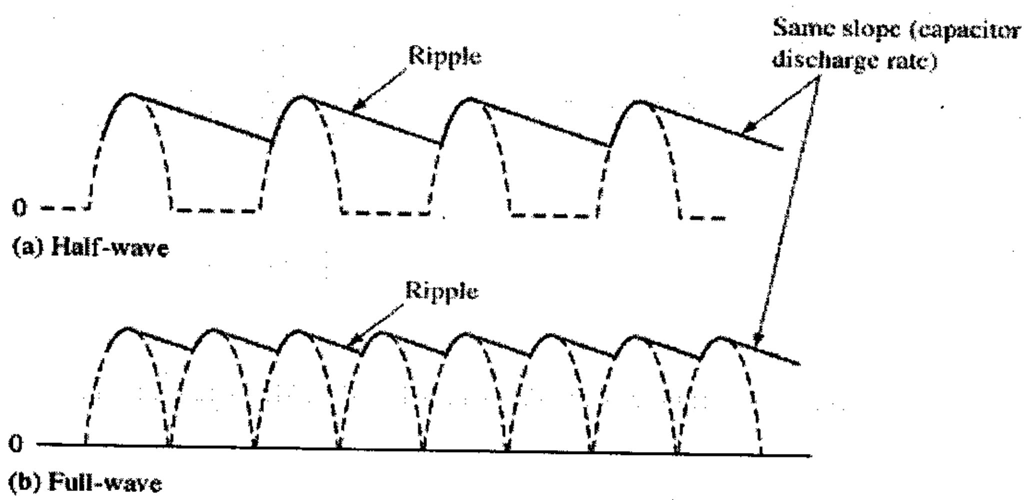
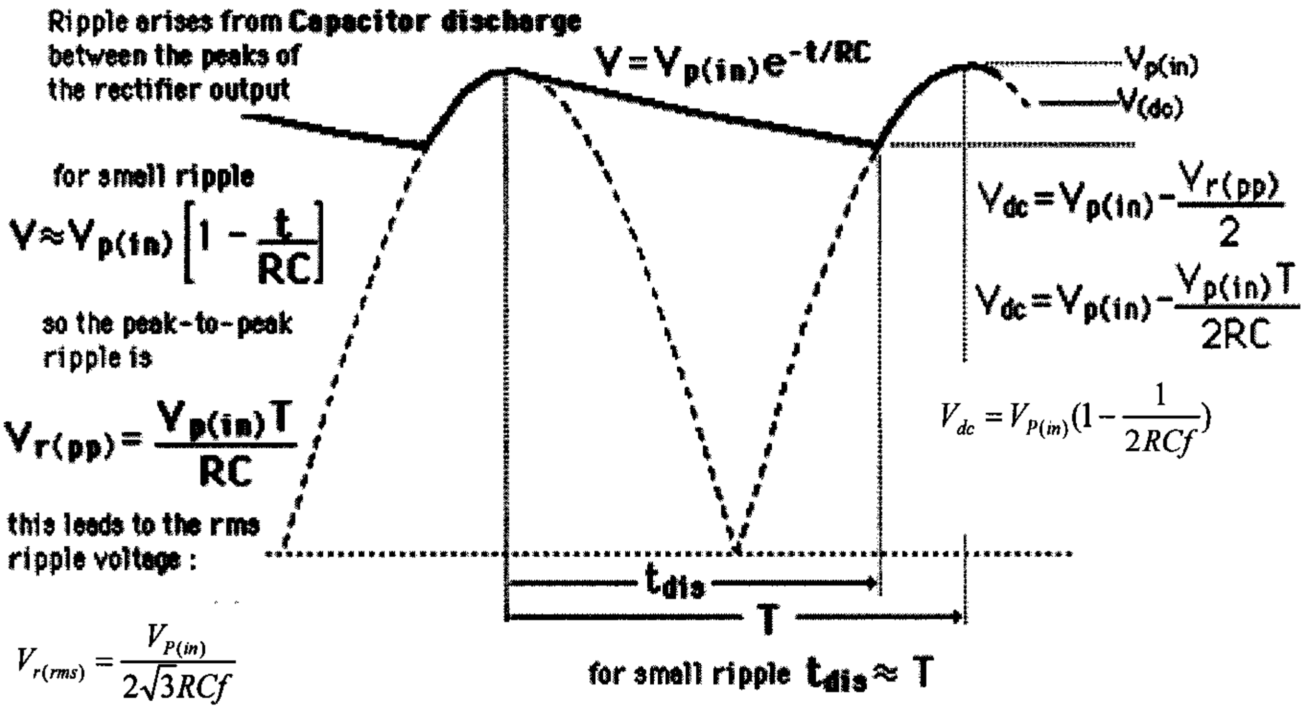


Fig.(22) the effect of regulator at a)HWR b) FWR circuit.



Hint/ f :frequency of input signal in HWR and double in FWR.

The ripple factor calculated by

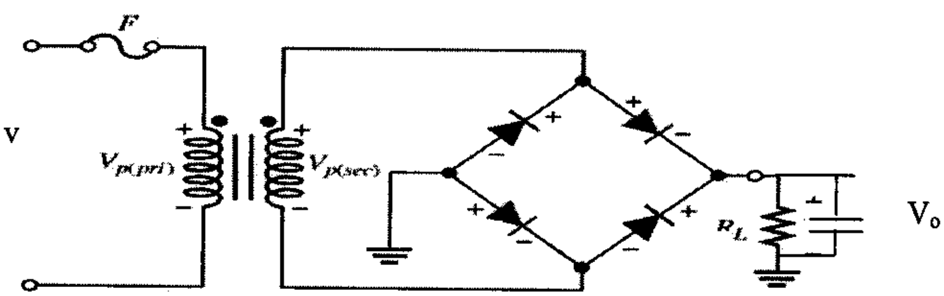
$$r = \frac{V_{r(rms)}}{V_{DC}}$$

$$r = \frac{1}{\sqrt{3}(2RCf - 1)}$$

Example/ The FWR cct. shown in Fig.() draw output wave form. Then find

i. DC voltage and current
ii. the ripple voltage
iii. ripple factor.
iv. Change in DC voltage if capacitor increased to 100 μF

$V_{in(rms)}$=220 v
f= 50 Hz



Ns/Np=1/5

R_L=10K Ω
C=50 μF

Sol/

$V_{in(p)}=V_{in(rms)} * \sqrt{2}$

$V_{in(p)}$= 311,13 volt

V_p= 311,13 *1/5 = 62,23 volt

F=2*50 =100 Hz

$$V_{dc} = V_{P(in)}(1-\frac{1}{2RCf})$$

$$V_{dc} = 61.6\ volt$$

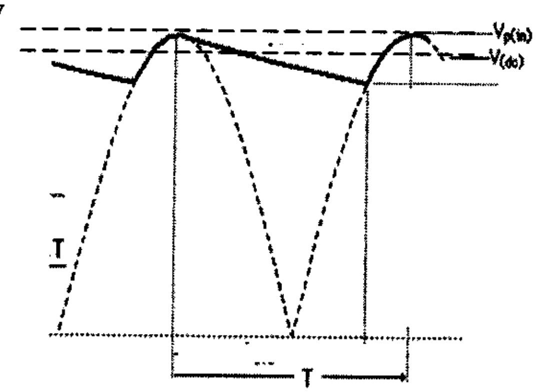
$$I_{dc} = \frac{V_{DC}}{R} = 6.16\ mA$$

$$r = \frac{1}{\sqrt{3}(2RCf-1)} = 5.77\%$$

$$r = \frac{V_{r(rms)}}{V_{DC}}$$

$$V_{r(rms)} = 0.3556\ volt$$

$$V_{r(PP)} = 1.232\ volt$$



T=1/100

iv. change capacitor 100 μF

$$V_{dc} = V_{P(in)}(1 - \frac{1}{2RCf})$$

$$V_{dc} = 61.92\ volt$$

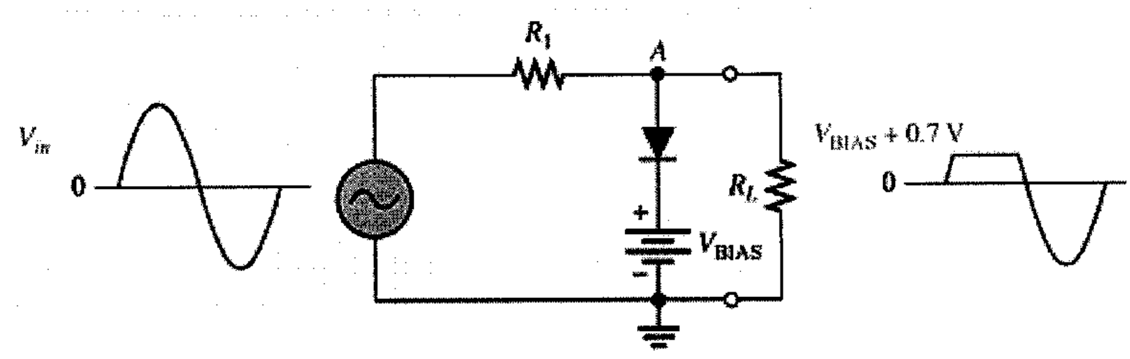
Change in DC voltage

61.92-61.6 = 0.32 volt

Q/ The HWR circuit with resistance load 20K and parallel capacitor C=100μF. If diode ideal calculate the DC voltage with and without capacitor, then draw the output wave if input signal **10 sin (t).**

4.2 Clipper

- Diodes can be used to clip off portions of signal voltages (above or below certain levels).
- Diode will become forward biased as soon as V_A becomes larger than V_{BIAS}+0.7.
- When diode is forward biased, V_A *cannot* become larger than V_{BIAS} + 0.7 V.
- Thus, the voltage across the load, R_L, will also be equal to V_{BIAS} + 0.7.
- When diode is reverse biased, it appears as an open, so the output voltage is the voltage of R_L alone.



Q/ Draw output wave form for two circuit below

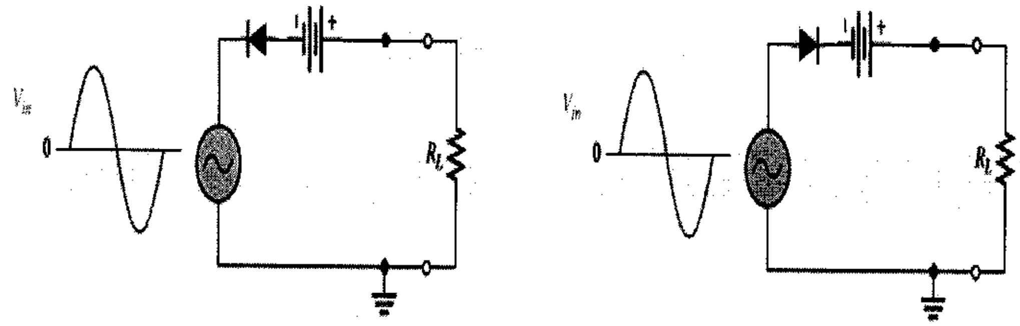


Fig.(23) The diode used as Clipper cct.

4.3 Diode Clampers

A clamper adds a dc level to an ac voltage, also called DC restorers. The clamper cct. shown in Fig. (24), analysis by

- When input voltage goes initially negative, diode is forward biased.
- Capacitor charges to near peak of inpt (Vp(in) – 0.7).
- Right after the negative peak, diode is reverse biased (because cathode is held near Vp(in) – 0.7 by charge on capacitor).
- Capacitor can only discharge through the RL.
- Since R_L has high resistance, the capacitor discharges very little each period.
- Note that time constant should be large (at least 10 times the period of the input voltage).
- Since capacitor retains charge, it acts like a battery in series with the input voltage.

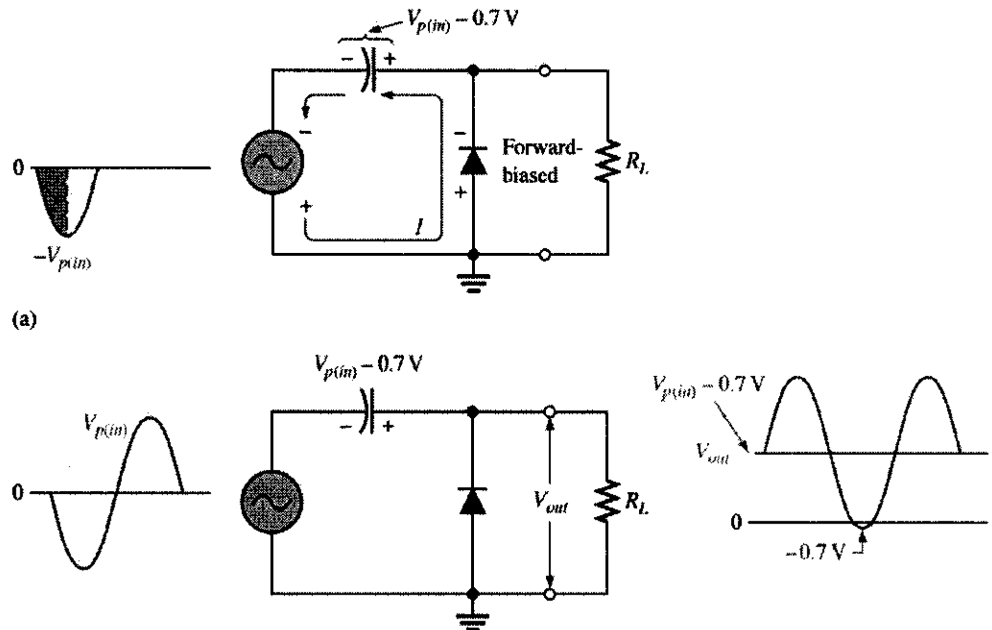
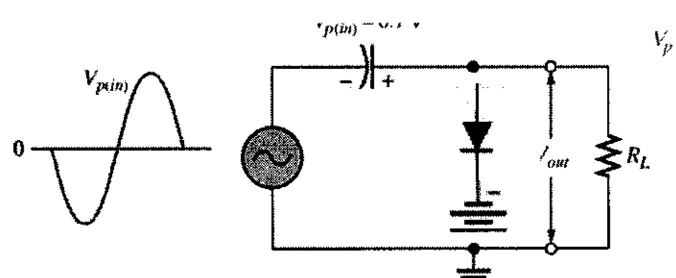


Fig.(24) The diode used as Clamper cct.

Q/ Draw output wave form for two circuit below



4.4DOUBLER

By use two diodes and two capacitor the cct. work as voltage doubler, as shown in Fig.(25). The cct. analysis is

- When secondary is positive, D_1 is forward biased and C_1 charges to approximately V_p.
- During the negative half-cycle, D_2 is forward biased and C_2 charges to approximately V_p.
- Output voltage is talked across the two capacitors in series.

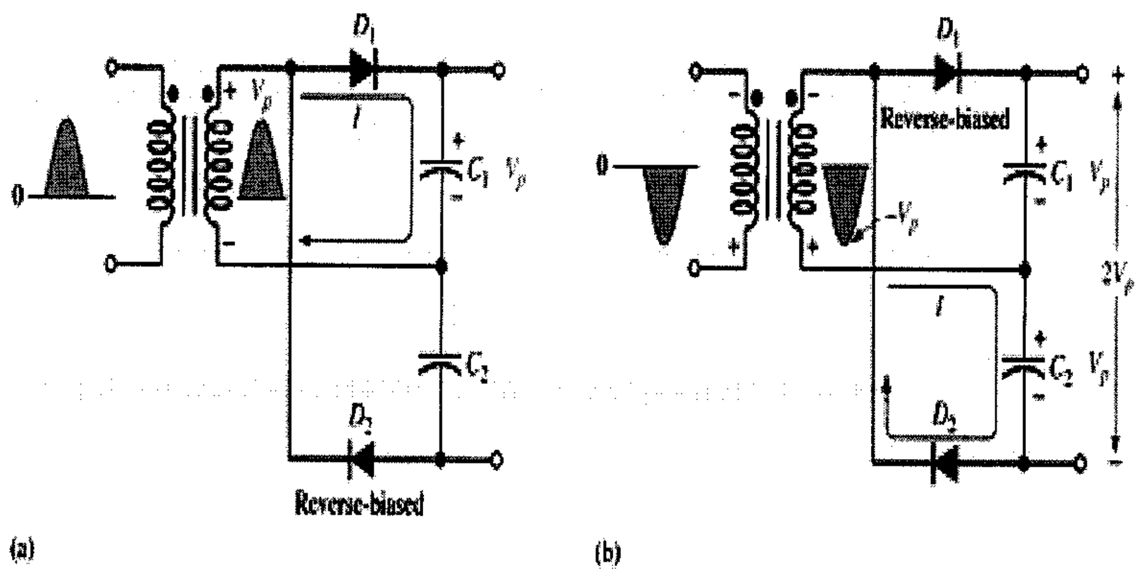


Fig.(25) The Voltage Double cct. a) Positive cycle b) Negative Cycle.

4.5 Zener Diodes

The analysis of circuit employing Zener diodes is equity similar to that applied to the semiconductor diode in F.B, if Zener diodes in R.B and the applied voltage across the diode greater than V_Z (Zener voltage), than the output voltage has been fixed at V_Z as shown in Fig.(26).

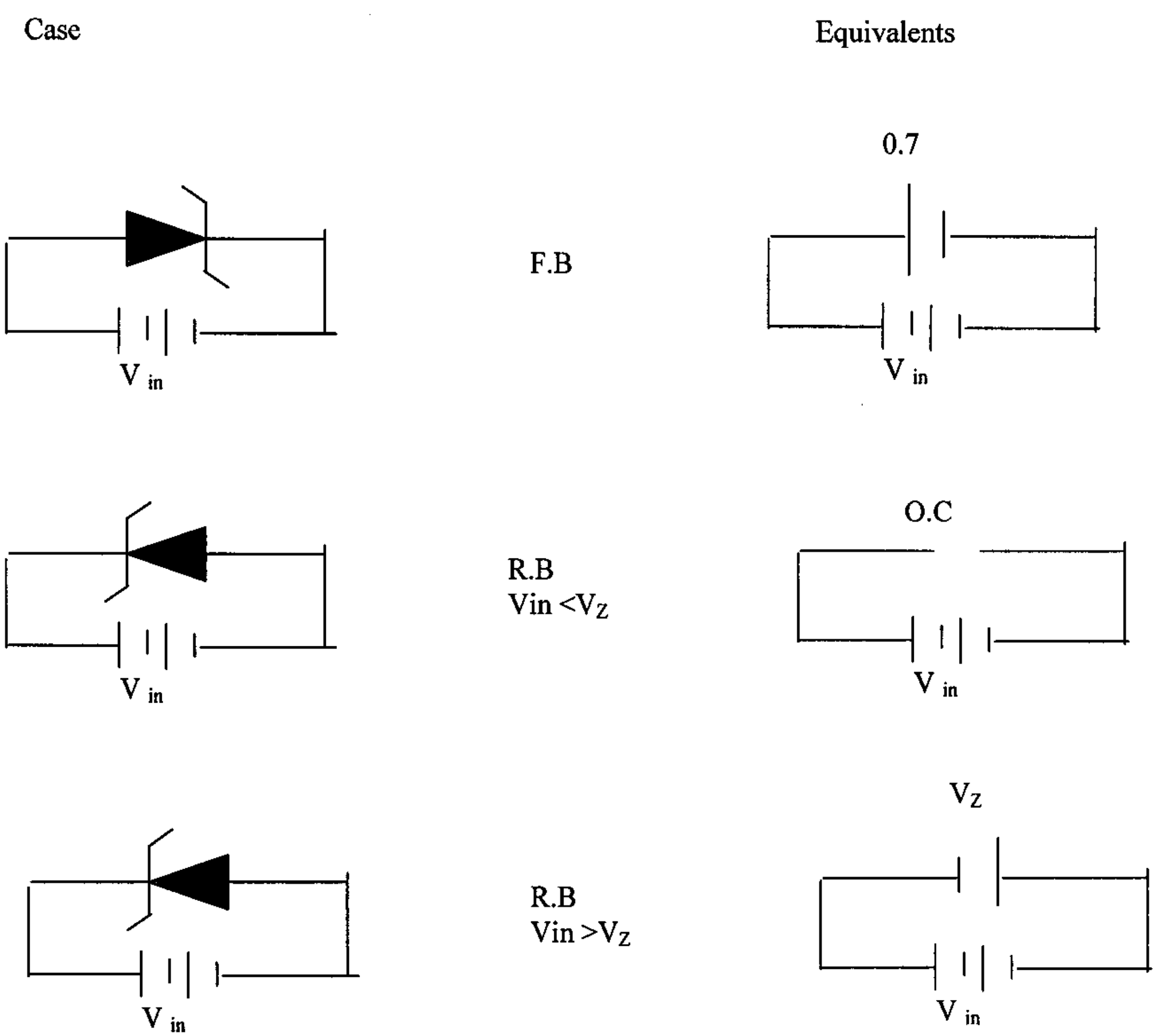


Fig.(26) the equivalent circuit of Zener Diode

For the three case shown in Fig. (26) the Zener Diodes Characteristics shown in Fig.(27)

Vin > V_Z Output voltge = V_Z ⟶ I_{Zmin} I_{Zmax}

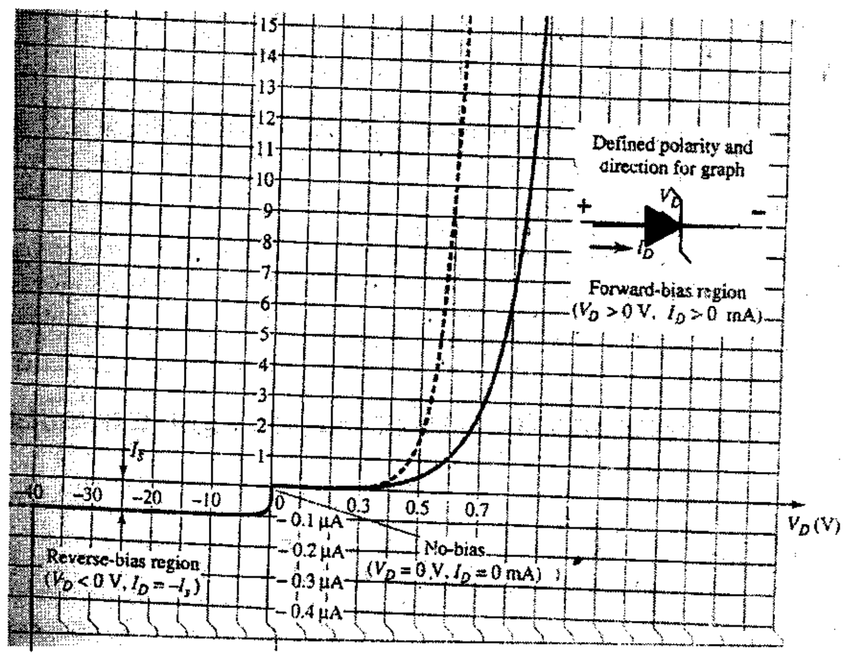


Fig.(27) Zener Diode Characteristic

4.5.1 Zener Diode as Voltage Regulator

The Zener diode in Fig. (28) works as voltage regulator, the load voltage has been fixed at V_Z when input voltage increase.

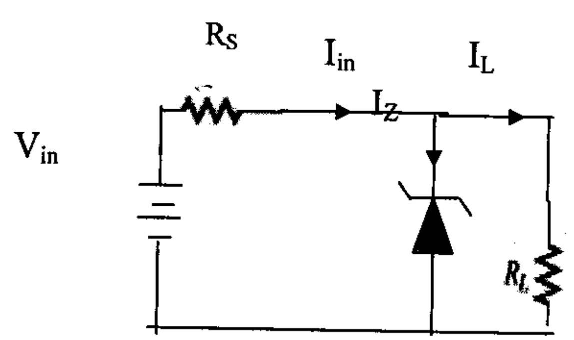


Fig.(28) Zener as voltage regulator

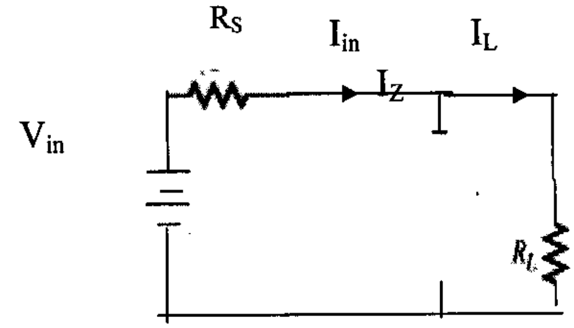
If $V_{in} < V_Z$

diode = o.c the equivalent cct. is

$$V_L = V_{in}\frac{R_L}{R_{Ls}+R_S}$$

$$I_Z = 0$$

$$I_{in} = I_L = \frac{V_{in}}{R_L+R_S} = \frac{V_{in}}{R_L}$$

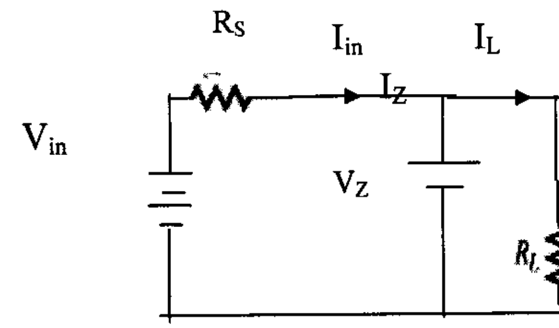


$$V_L = V_Z$$

$$I_L = \frac{V_Z}{R_L}$$

$$I_{in} = I_L + I_Z$$

$$\frac{V_{in}}{R_L+R_S} = \frac{V_Z}{R_L} + I_Z$$



P_Z: Total dissipated power in Zener diode is

$$P_z = V_Z . I_Z$$

4.5.2 Variable load (R_L) with fixed (V_{in})

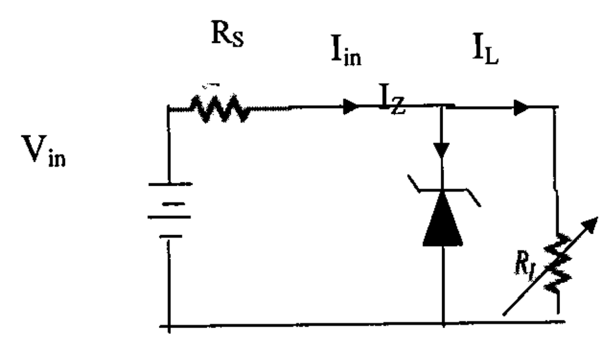
Due to V_Z there is a specific range of resistance value which will ensure that Zener is in the ON state. The R_{Lmin} result of load voltage be less Zener voltage and Zener device have min Zener current I_{Zmin}. When R_{Lmax} that result increasing in load current and Zener siode have max current I_{Zmax}. $R_{Lmin} < R_L < R_{Lmax}$

$$I_{in} = I_L + I_Z$$

$$I_{in} = \frac{V_{in}-V_z}{R_S} \qquad I_L = \frac{V_Z}{R_{L\,min}}$$

$$\frac{V_{in}-V_z}{R_S} = \frac{V_Z}{R_{L\,min}} + I_{Z\,min}$$

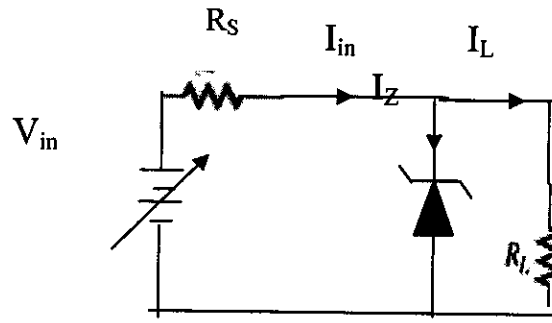
$$\frac{V_{in}-V_z}{R_S} = \frac{V_Z}{R_{L\,max}} + I_{Z\,max}$$



4.5.3 Variable (V_{in}) with fixed (R_L)

If R_L fixed then the input voltage V_{in} must be sufficiently large to turn the Zener diode ON. The Vin_{min} turn with min Zener current I_{Zmin}. When Vin_{max} turn with Zener diode have max current I_{Zmax}, that result an fixed load current I_L.

$Vin_{min} < Vin < Vin_{max}$



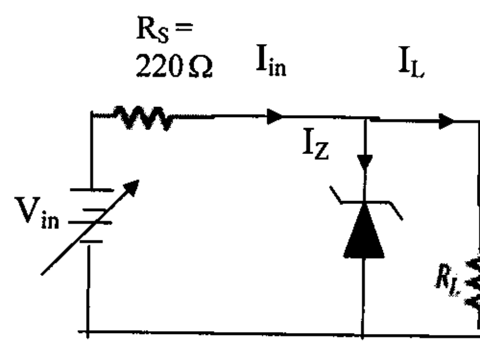
$$I_{in} = I_L + I_Z$$

$$I_{in_{min}} = \frac{V_{in_{min}} - V_z}{R_S} \qquad I_L = \frac{V_Z}{R_L}$$

$$\frac{V_{in_{min}} - V_z}{R_S} = \frac{V_Z}{R_L} + I_{Z\,min}$$

$$\frac{V_{in_{min}} - V_z}{R_S} = \frac{V_Z}{R_L} + I_{Z\,max}$$

Example / Determined the range of values for V_{in} that will maintain the Zener diode in ON state, for the cct. shown below



$V_Z = 20V$ $\quad R_L = 1.2K\Omega$
$I_{Zmax} = 60mA$
$I_{Zmin} = 0$

SOL/

$$I_{in} = I_L + I_Z$$

$$I_{in_{min}} = \frac{V_{in_{min}} - V_z}{R_S} \qquad I_L = \frac{V_Z}{R_L}$$

$$\frac{V_{in_{min}} - V_z}{R_S} = \frac{V_Z}{R_L} + I_{Z\,min}$$

$$\frac{V_{in_{min}} - 20}{220} = \frac{20}{1200} + 0$$

$$V_{in_{min}} = 23.6\ volt$$

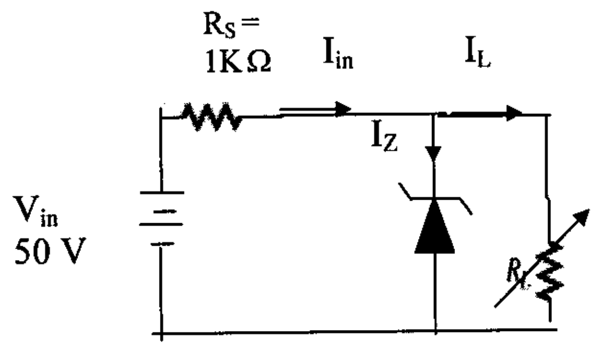
$$\frac{V_{in_{min}} - V_z}{R_S} = \frac{V_Z}{R_L} + I_{Z\max}$$

$$\frac{V_{in_{min}} - 20}{220} = \frac{20}{1200} + 60*10^{-3}$$

$$V_{in_{min}} = 36.87 \ volt$$

$$23.6 \le V_{in} \le 36.87 \ volt$$

Example / Determined the range of values fo R_L that will maintain the Zener diode in ON state, for the cct. shown below



$V_Z = 10V$
$I_{Zmax} = 32mA$
$I_{Zmin} = 0$

SOL/

$$I_{in} = I_L + I_Z$$

$$I_{in} = \frac{V_{in} - V_z}{R_S} \qquad I_L = \frac{V_Z}{R_{L\min}}$$

$$\frac{V_{in} - V_z}{R_S} = \frac{V_Z}{R_L} + I_{Z\min}$$

$$\frac{50 - 20}{1000} = \frac{10}{R_{L\min}} + 0$$

$$R_{L\min} = 250 \ \Omega$$

$$\frac{V_{in} - V_z}{R_S} = \frac{V_Z}{R_{L\max}} + I_{Z\max}$$

$$\frac{50 - 20}{1000} = \frac{10}{R_{L\min}} + 32*10^{-3}$$

$$R_{L\min} = 1250 \ \Omega$$

$$250 \le R_L \le 1250 \ \Omega$$

Q/ The DC voltage supply have V_{in} =50 volt used in regulator cct. contian Zener diode, the load voltage fixed at V_L=12 volt and load current change from (10mA-200mA). Design the cct. then determined R_S, V_z, and $P_{Z\ max}$.

5. Bipolar Junction Transistor

5.1 BJT Structure and Operator

The transistor is a three layer semiconductor device consisting of two N-type and one P-type layers of material call (NPN) transistor or two P-type and one N-type layers of material call (PNP) transistor as shown in Fig.(29). In transistor two depletion region have made between three layers, that's name

E : Emitter (High doping layer and wide width)

C: Collector (Low doping layer but wide width)

B: Base (Low doping layer the ratio of width depend on Emitter 150:1)

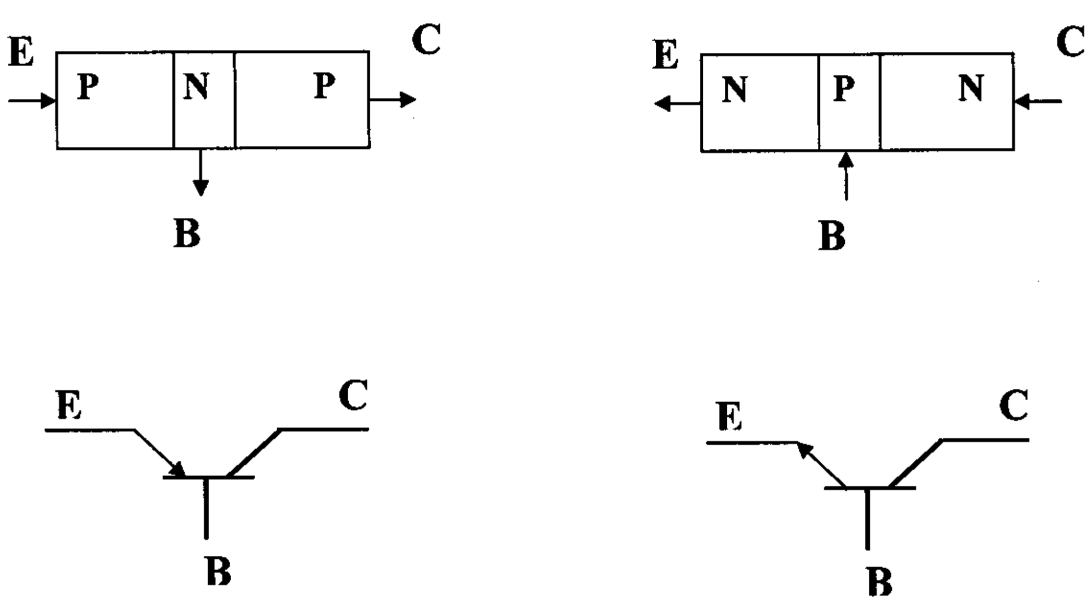


Fig.(29) The BJT transistor
a) PNP transistor with symbol
b) NPN transistor with symbol.

The basic operation of the transistor (PNP) as shown in Fig.(30)

- J_1 (junction one) between Emitter and Base is F.B, the depletion region reduced. Large Hole current has been passed.
- J_2 (junction Two) between Collector and Base is R.B, the depletion region wide. The current pass only the minority carrier.

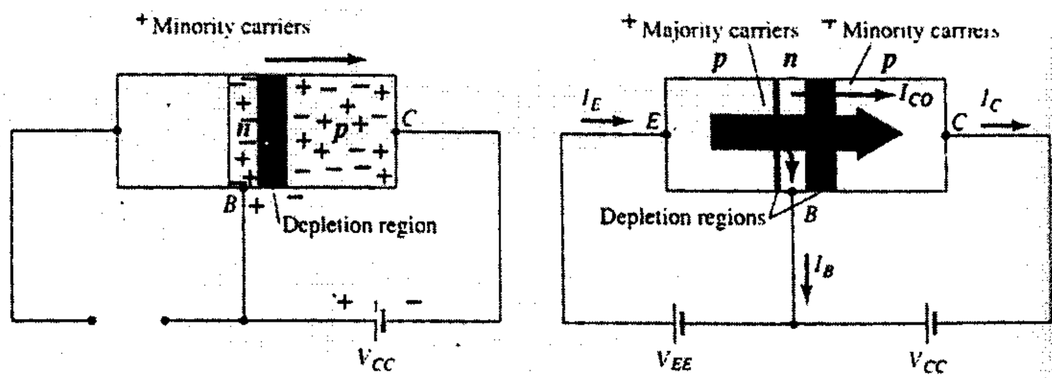


Fig.(30) Transistor Bias

By apply Kerchief Current low the transistor currents as shown in Fig.(31) are

$$I_E = I_C + I_B$$

I_E: Emitter current

I_C: Collector Current

I_B: Base Current

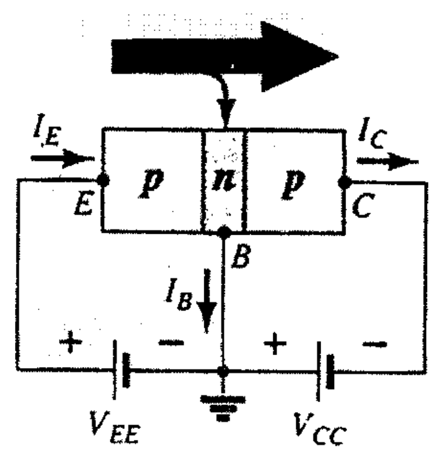
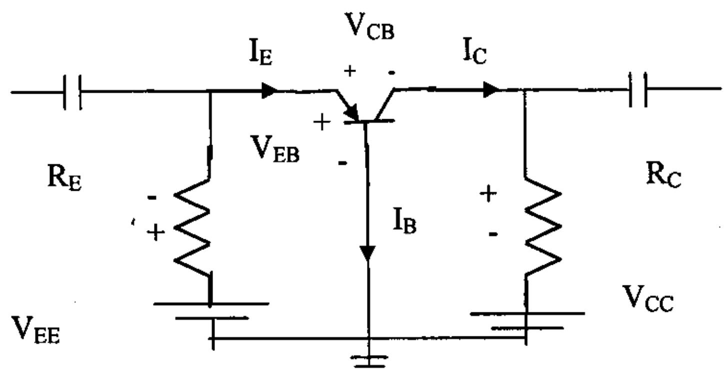


Fig.(31) BJT transistor Currents.

5.2 Common-Base Configuration

The Common-Base configuration set Emitter as input port and Collector as output port and base as common for that call C.B.



C.B input port

Input current I_E

Input voltage V_{EB}

C.B output port

output current I_C

output voltage V_{CB}

the relation ship between input and output current depend on α coefficient

$$I_C = \alpha \ I_E$$

The input characteristic of C.B transistor shown in Fig.(32), the input curve (between current I_E and voltage V_{EB}) various when output voltage change.

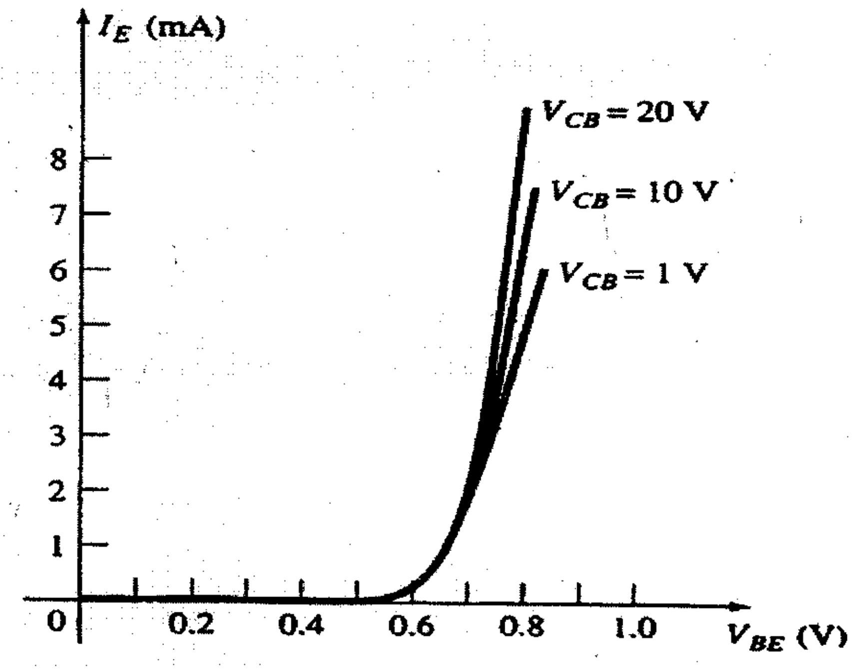


Fig.(32) Input Characteristic of C.B transistor.

The output characteristic of C.B transistor shown in Fig.(33), the output curve (between current I_C and voltage V_{CB}) various when input current change.

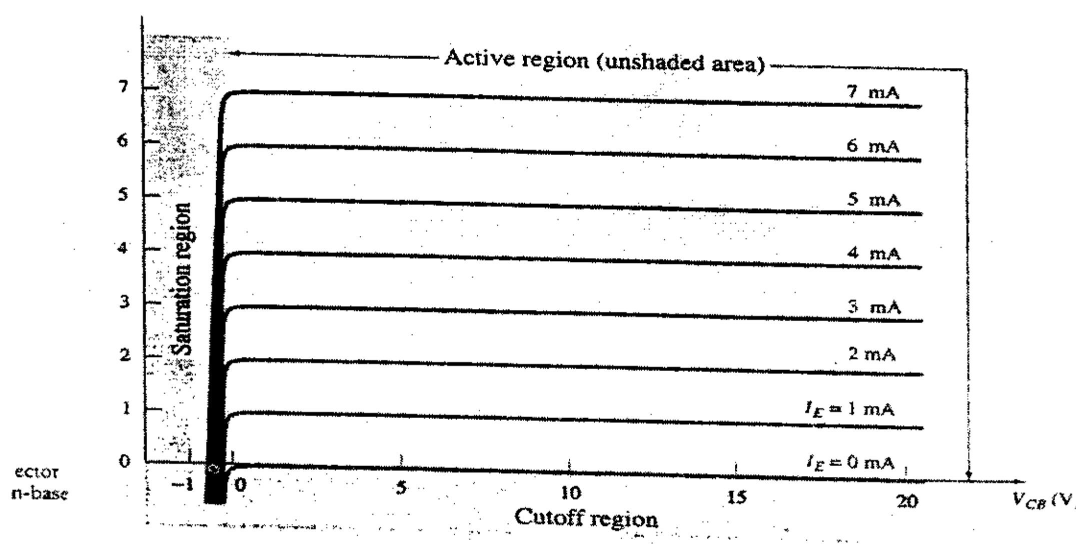


Fig.(33) Output Characteristic of C.B transistor.

- Common-Base Analysis

The C.B circuit shown below analyzed by two loop

- input loop

$V_{EE} - I_E R_E - V_{EB} = 0$

Emitter-Base junction F.B then $V_{EB} = 0.7$ volt in (PNP)

$V_{BE} = 0.7$ volt in (NPN)

$$I_E = \frac{V_{EE} - V_{EB}}{R_E}$$

$$I_C = \alpha I_E$$

- output loop

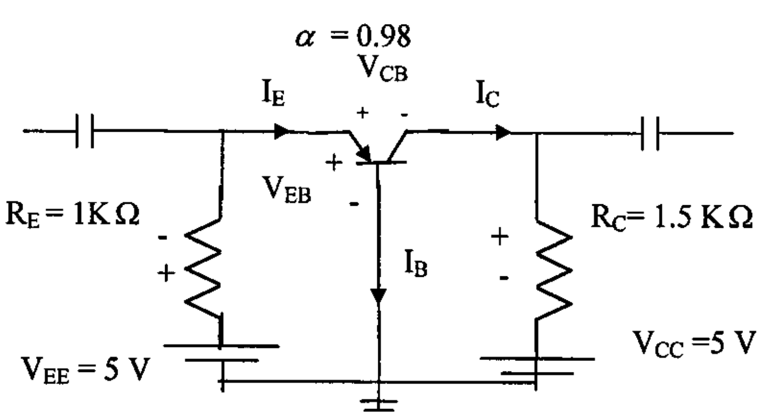
$$V_{CC} + I_C R_C - V_{CB} = 0$$

$$V_{CB} = V_{CC} + I_C R_C$$

Q- point (the transistor work point)

Q (V_{CB}, I_C)

Example/ The electron circuit shown below find Q point



SOL/

$$I_E = \frac{V_{EE} - V_{EB}}{R_E} = \frac{5 - 0.7}{1000} = 4.3\ mA$$

$$I_C = \alpha I_E = 0.98 * 4.3 * 10^{-3} = 4.214\ mA$$

$V_{CC} + I_C R_C - V_{CB} = 0$

$V_{CB} = V_{CC} + I_C R_C$

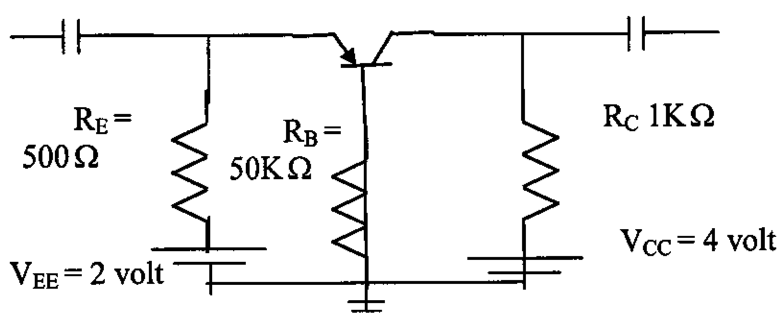
$V_{CB} = 7 + 4.214 * 10^{-3} * 1.5 * 10^{3}$

$V_{CB} = 12.321\ volt$

Q point (V_{CB} = 12.321 volt , I_C = 4.214 mA)

Q/ The electron circuit shown below find Q point, I_E, I_C, I_B, V_E, and V_C

α =0.98



4.1 Common Emitter Configuration

The Common-Emitter configuration set Base as input port and Collector as output port and Emitter as common for that call C.E.

C.E input port

Input current I_B

Input voltage V_{BE}

C.E output port

output current I_C

output voltage V_{CE}

the relation ship between input and output current depend on β coefficient

$$I_C = \beta\, I_B$$

The input characteristic of C.E transistor shown in Fig.(34), the input curve (between current I_B and voltage V_{BE}) various when output voltage change.

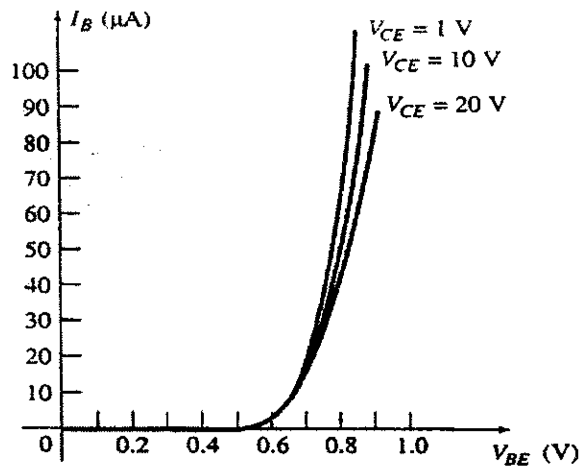


Fig.(34) Input Characteristic of C.E transistor.

The output characteristic of C.E transistor shown in Fig.(35), the output curve (between current I_C and voltage V_{CE}) various when input current change.

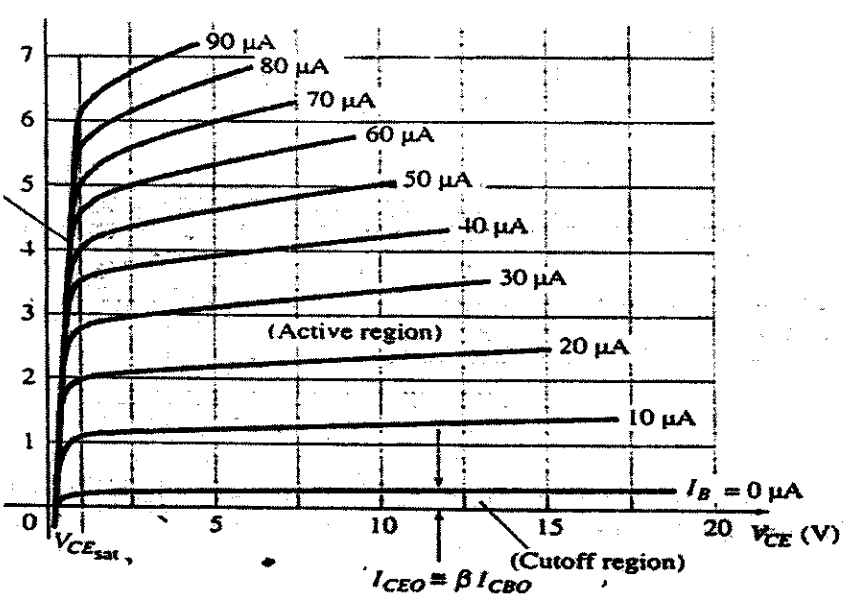


Fig.(35) Output Characteristic of C.E transistor.

- **The relation ship between α *and* β**

$$I_E = I_C + I_B$$
$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$
$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$
$$\alpha = \frac{\beta}{1+\beta}$$

anotherrelashion

$$\frac{1}{\beta} = 1 - \frac{1}{\alpha}$$
$$\beta = \frac{\alpha}{\alpha - 1}$$

The relation Between I_E and I_B

$I_E = (\beta + 1)\, I_B$

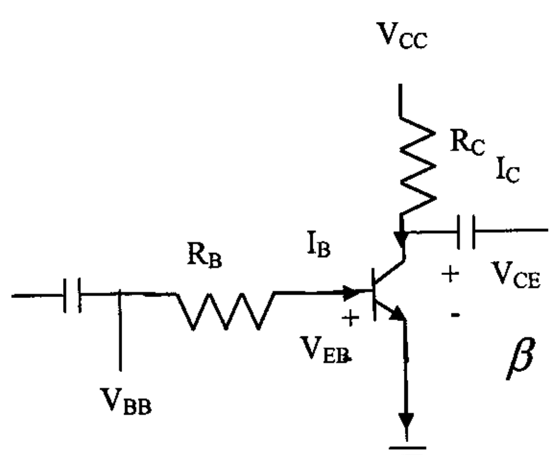
- **Analysis of C.E Transistor**

- input loop

$V_{BB} - I_B R_B - V_{BE} = 0$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$
$$I_C = \beta I_B$$

- output loop



$$V_{CC} - I_C R_C - V_{CE} = 0$$
$$V_{CE} = V_{CC} - I_C R_C$$

Q- point (the transistor work point)

Q (V_{CE}, I_C)

- Load Line and Transistor Regions

The load line analysis is he sum of points that transistor can work on it in different type of input current I_B. To draw Load line two region must be calculated

1- Cutoff Region

Where both junction of transistor are R.B the currents pass through transistor are Zeros

$I_C = I_B = 0$

From output loop can calculate V_{CE} in cutoff

$$V_{CC} - I_C R_C - V_{CE} = 0 \qquad I_C = 0$$
$$V_{CE}(cutoff) = V_{CC}$$

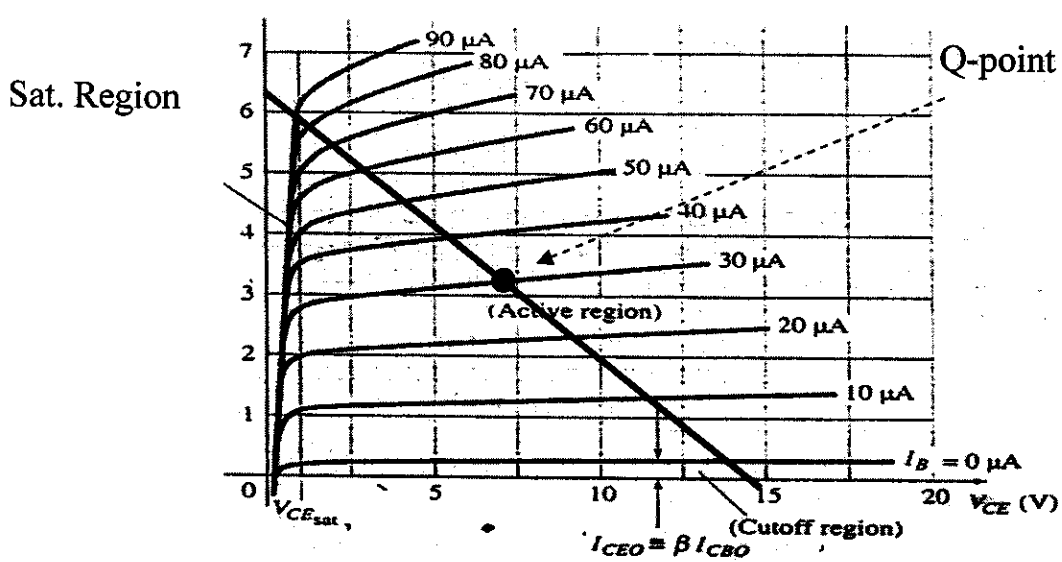
2- Saturation Region

Where both junction of transistor are F.B the currents pass through transistor are the maximum current hold from transistor

$V_{CE} = 0$ (practical 0.2 volt)

From output loop can calculate $I_{C(sat.)}$ is

$$V_{CC} - I_C R_C - V_{CE} = 0 \qquad V_{CE} = 0$$
$$I_C(Sat.) = \frac{V_{CC}}{R_C}$$



- C. E with R_E

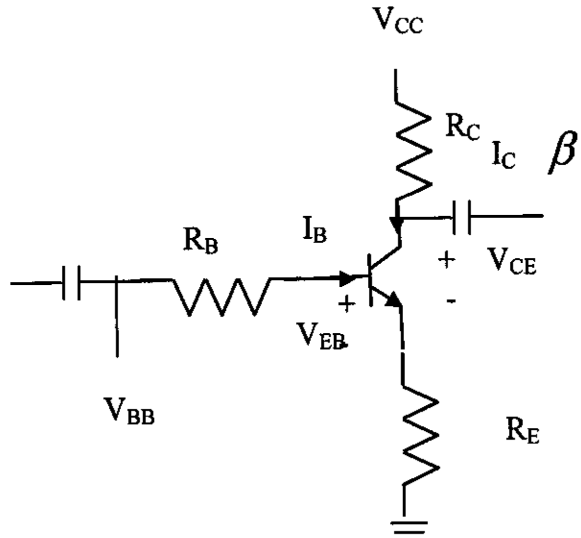
In this cct. an R_E resistance are connect between Emitter and Earth, this resistance gives more stability to Q-point when β change.

- input loop

$V_{BB} - I_B R_B - V_{BE} - I_E R_E = 0$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$I_C = \beta I_B$



output loop

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$I_C \approx I_E$

$V_{CE} = V_{CC} - I_C(R_C + R_E)$

Q- point (the transistor work point)

Q (V_{CE}, I_C)

Example/ for the cct. shown below Find Q. point for β=50 and 80

Sol/

For β=50

$V_{BB} - I_B R_B - V_{BE} - I_E R_E = 0$

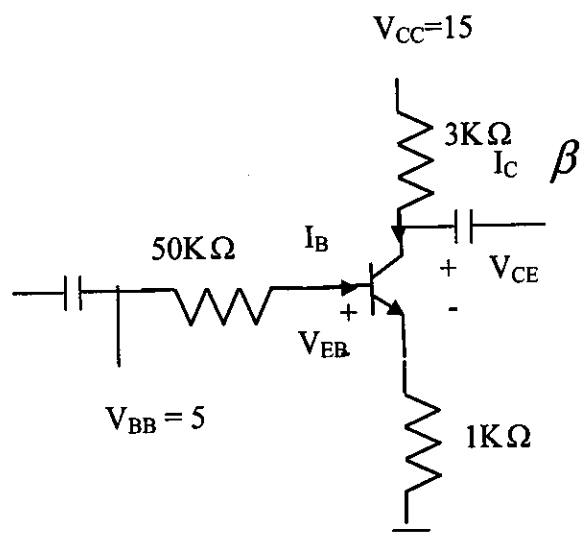
$$I_B = \frac{5 - 0.7}{50 * 10^3 + (50 + 1)1000} = 43\ \mu A$$

$I_C = \beta I_B = 2.15\ mA$

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$V_{CE} = 15 - 2.15 * 10^{-3} * (3 * 10^3 + 1 * 10^3)$

$V_{CE} = 6.4\ volt$



For β=80

$V_{BB} - I_B R_B - V_{BE} - I_E R_E = 0$

$$I_B = \frac{5-0.7}{50*10^3 + (80+1)1000} = 32.8\ \mu A$$

$$I_C = \beta I_B = 2.63\ mA$$

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = 15 - 2.63*10^{-3}*(3*10^3 + 1*10^3)$$

$$V_{CE} = 4.48\ volt$$

For β=50 (**V_{CE}** = 6.4 volt , **I_C** = 2.15 mA)

For β=80 (**V_{CE}** = 4.48 volt , **I_C** = 2.63 mA)

- C. E Self Bias

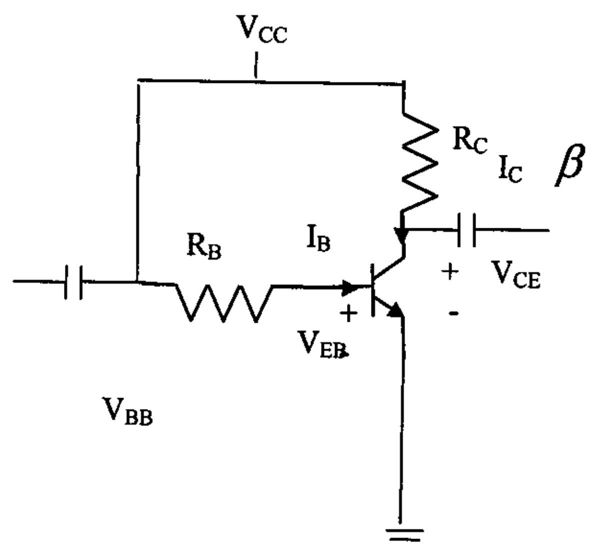
In this cct. only one suppliy used to bias the two junctions.

- input loop

$V_{CC} - I_B R_B - V_{BE} = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B$$



- output loop

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

Q (V_{CE}, I_C)

- C. E Self Bias with R_E

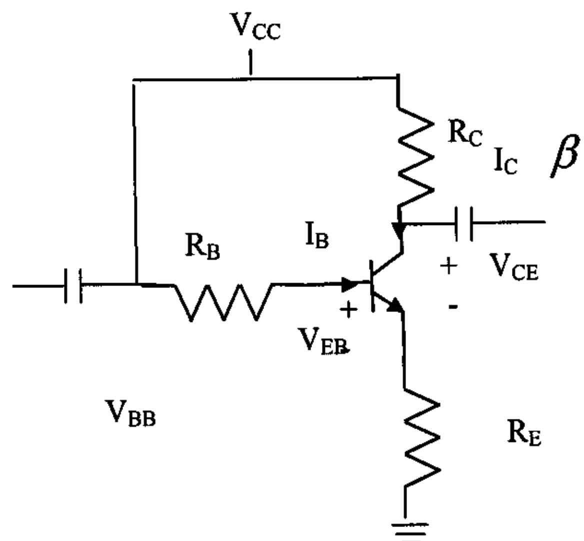
In this cct. an R_E resistance are connect between Emitter and Earth

- input loop

$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$I_C = \beta I_B$



- output loop

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$I_C \approx I_E$

$V_{CE} = V_{CC} - I_C(R_C + R_E)$

Q (V_{CE}, I_C)

Example/ for the cct. shown below Find Q. point for β=30 and 60

Sol/

For β=30

$V_{BB} - I_B R_B - V_{BE} - I_E R_E = 0$

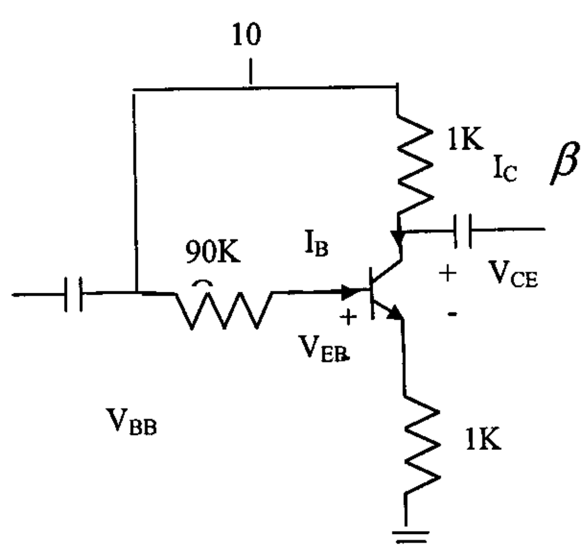
$$I_B = \frac{10 - 0.7}{90 * 10^3 + (30 + 1) * 1 * 10^3} = 76.8\ \mu A$$

$I_C = \beta I_B = 2.3\ mA$

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$V_{CE} = 10 - 2.3 * 10^{-3} * (1 * 10^3 + 1 * 10^3)$

$V_{CE} = 5.4\ volt$



For β=60

$$I_B = \frac{10 - 0.7}{90 * 10^3 + (60 + 1) * 1 * 10^3} = 71\ \mu A$$

$I_C = \beta I_B = 4.26\ mA$

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

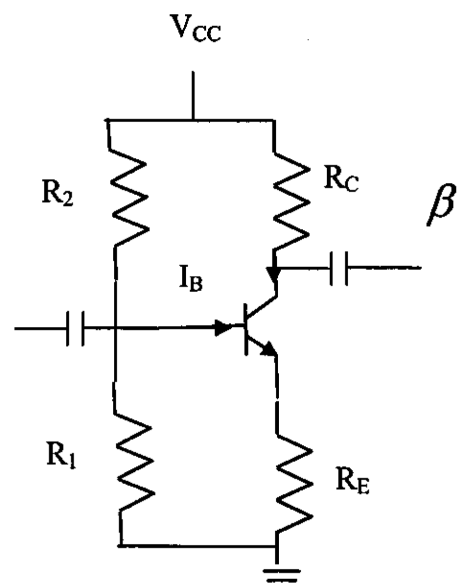
$V_{CE} = 10 - 4.26 * 10^{-3} * (1 * 10^3 + 1 * 10^3)$

$V_{CE} = 1.48$ *volt*

For β**=30** (V_{CE} = 5.4 volt , I_C = 2.3 mA)

For β**=60** (V_{CE} = 1.48 volt , I_C = 4.26 mA)

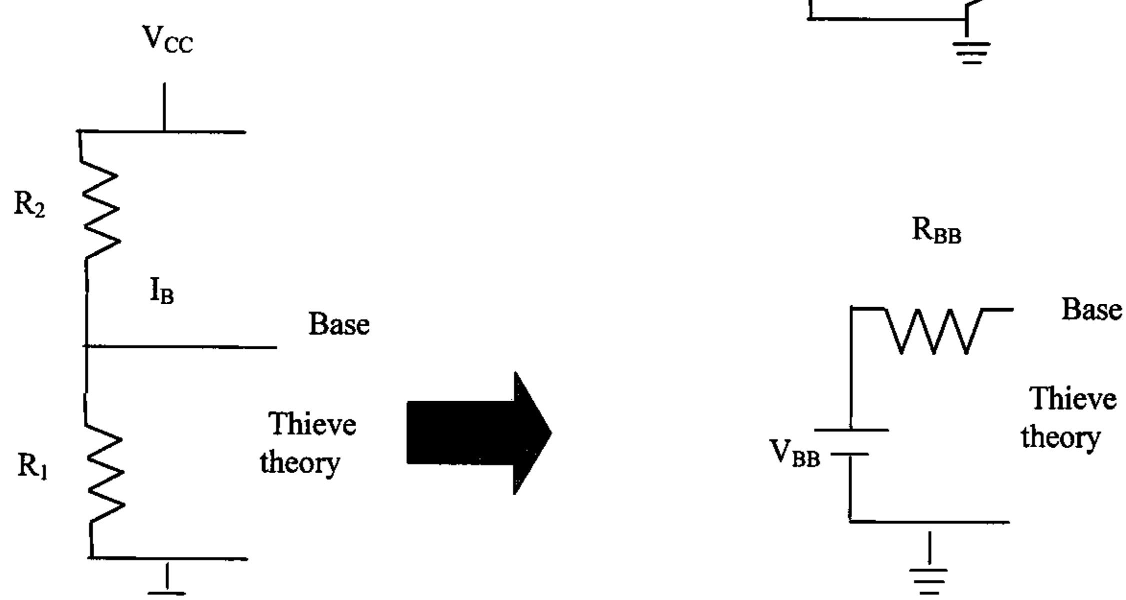
In this cct. increase β **100%** change I_C by **70%**



- An Dependent of β **Circuit**

This cct. used two resistance in input loop, this give part of V_{CC} in input voltage.

By using thieven theory in input loop to find V_{BB} and R_{BB}



$$V_{BB} = V_{CC} \frac{R_1}{R_1 + R_2} \qquad R_{BB} = \frac{R_1 \ R_2}{R_1 + R_2}$$

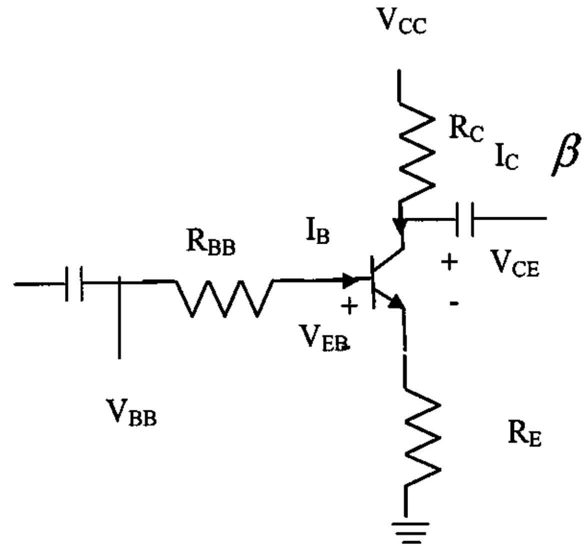
- input loop

$V_{BB} - I_B R_{BB} - V_{BE} - I_E R_E = 0$

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB} + (\beta + 1)R_E}$$

$$I_C = \beta I_B$$

- output loop



$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

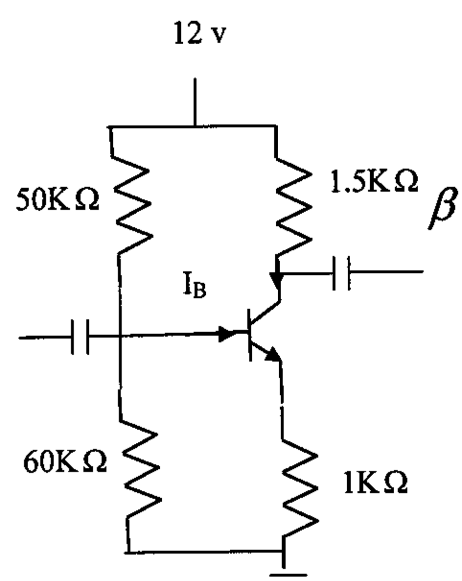
$$I_C \approx I_E$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Q- point Q (V_{CE}, I_C)

Example/ for the cct. shown below Find Q. point for β=50 and 70

SOL/



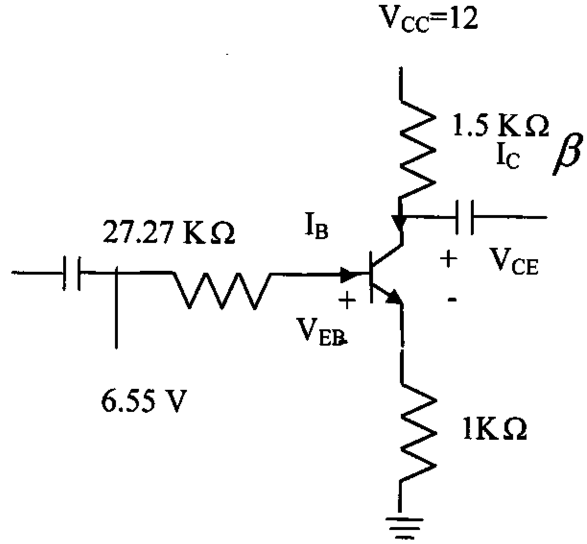
$$R_{BB} = \frac{R_1 R_2}{R_1 + R_2}$$

$$R_{BB} = \frac{50*10^3 * 60*10^3}{50*10^3 + 60*10^3} = 27.27 \ K\Omega$$

$$V_{BB} = V_{CC}\frac{R_1}{R_1 + R_2}$$

$$V_{BB} = 12\frac{60*10^3}{50*10^3 + 60*10^3} = 6.55 \ volt$$

For β=50



$V_{BB} - I_B R_{BB} - V_{BE} - I_E R_E = 0$

$$I_B = \frac{6.55-0.7}{27.27*10^3+(50+1)1000} = 73.3\ \mu A$$

$I_C = \beta I_B = 3.72\ mA$

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$V_{CE} = 12 - 3.72*10^{-3}*(1.5*10^3 + 1*10^3)$

$V_{CE} = 2.71\ volt$

For β=70

$V_{BB} - I_B R_{BB} - V_{BE} - I_E R_E = 0$

$$I_B = \frac{6.55-0.7}{27.27*10^3+(70+1)1000} = 59.3\ \mu A$$

$I_C = \beta I_B = 4.15\ mA$

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$V_{CE} = 12 - 4.15*10^{-3}*(1.5*10^3 + 1*10^3)$

$V_{CE} = 1.62\ volt$

For β=50 (V_{CE} = 2.71 volt , I_C = 3.72 mA)

For β=70 (V_{CE} = 1.62 volt , I_C = 4.15 mA)

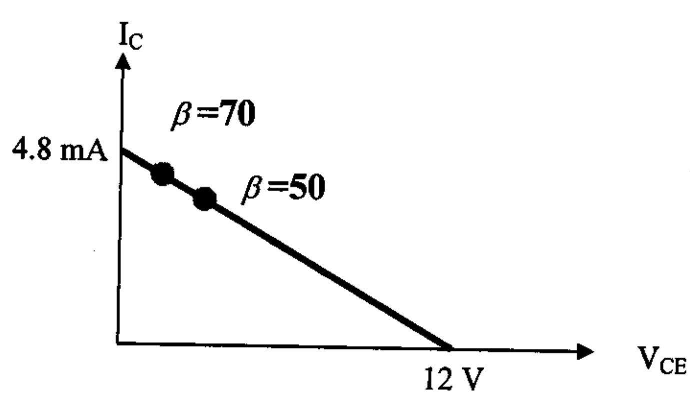
Load line

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$ (output loop)

$12 - I_C(2.5*10^3) - V_{CE} = 0$

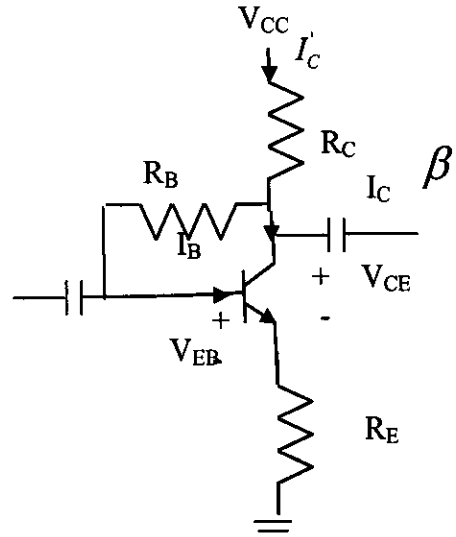
Cutoff Region $I_C = 0$ VCE =12 volt

Saturation Region $V_{CE} = 0$ $I_{C(Sat)} = 4.8$ mA



- C.E with Feedback Resistance

- input loop



$$I_C' = I_C + I_B$$
$$I_C' = I_E$$
$$V_{CC} - I_E R_C - I_B R_{BB} - V_{BE} - I_E R_E = 0$$
$$I_B = \frac{V_{CC} - V_{BE}}{R_{BB} + (\beta + 1)(R_E + R_C)}$$
$$I_C = \beta I_B$$

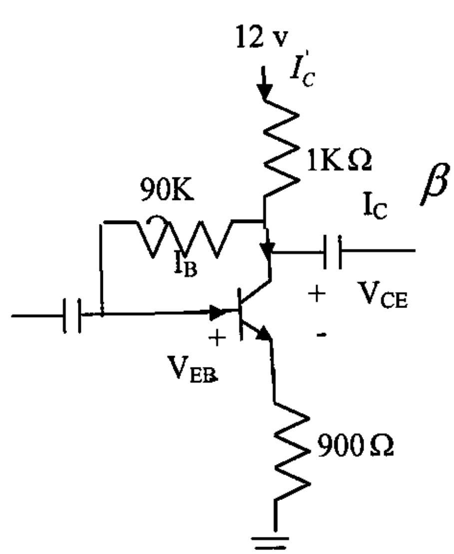
- output loop

$$V_{CC} - I_E R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C \frac{(R_C + R_E)}{\alpha}$$

Q- point Q (V_{CE}, I_C)

Q / for the cct. shown below Find Q. point for β=50 and 70



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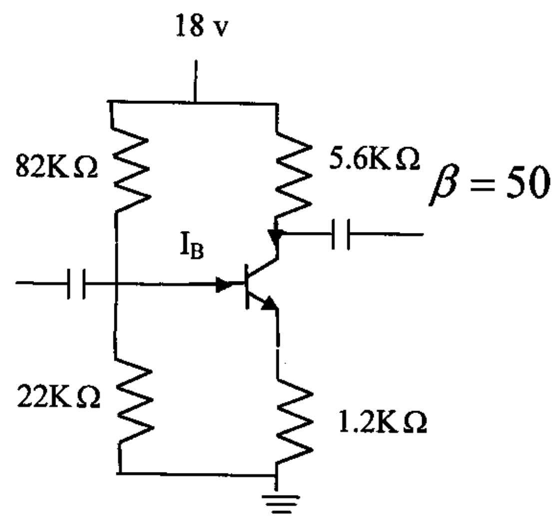
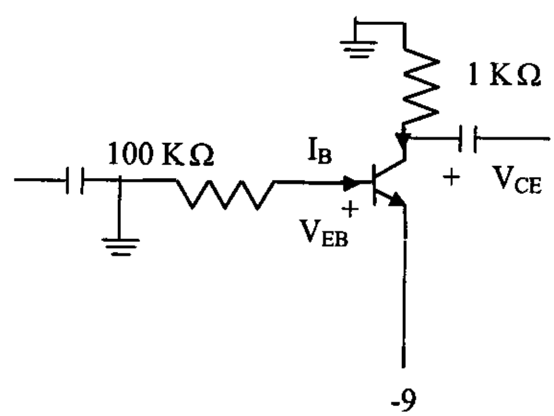
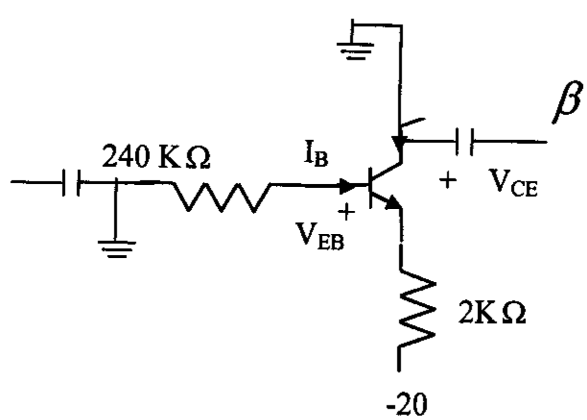
Q1 / for the cct. shown below Find Q. point, load line, V_B, V_C, and V_{CB}



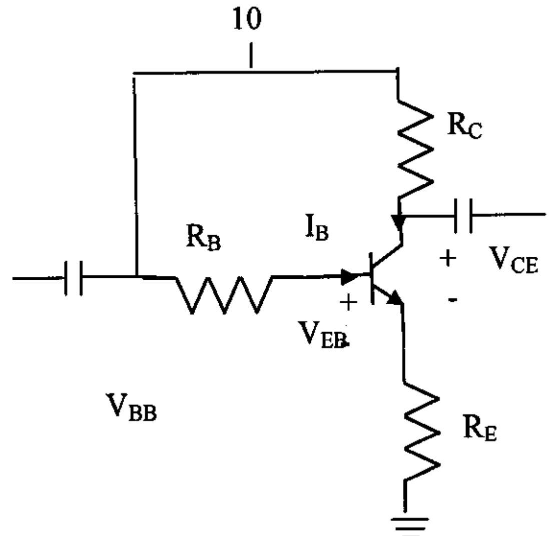
Q2 / for the cct. shown below Find Q. point and load line



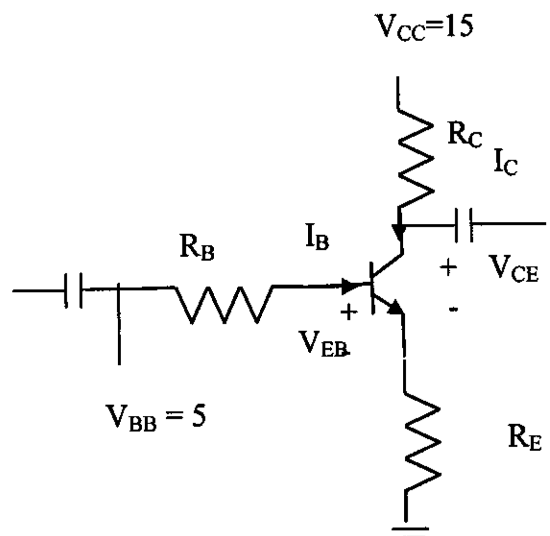
Q3 / for the cct. shown below Find Q. point and load line



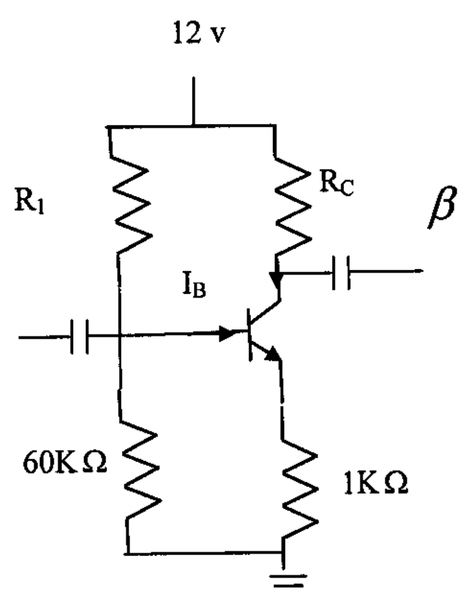
Q4/ for the cct. shown below Find R_B, R_C, and R_E . If β=30, V_{CE} = 5.4 volt , I_C = 2.3 mA, and V_E = 2.31 Volt.



Q5/ for the cct. shown below Find R_B, R_C, and R_E . If β=50, V_{CE} = 6.4 volt , I_C = 2.15 mA, and V_E = 2.2 Volt.
Calculate change in Q.point if V_{BB} = 9 volt.



Q6/ for the cct. shown below Q. point (5.4 V, 2.3 mA) and β=50.
Find R_C and R_1.



6.The Field-Effect Transistor (FET)

The ***bipolar junction transistor BJT current Controlled current device (CCCD) when FET Field Effect Transistor voltage controlled current device (VCCD).*** The output current of the FET is controlled by an input voltage, not an input current. There are two basic types of FET's:

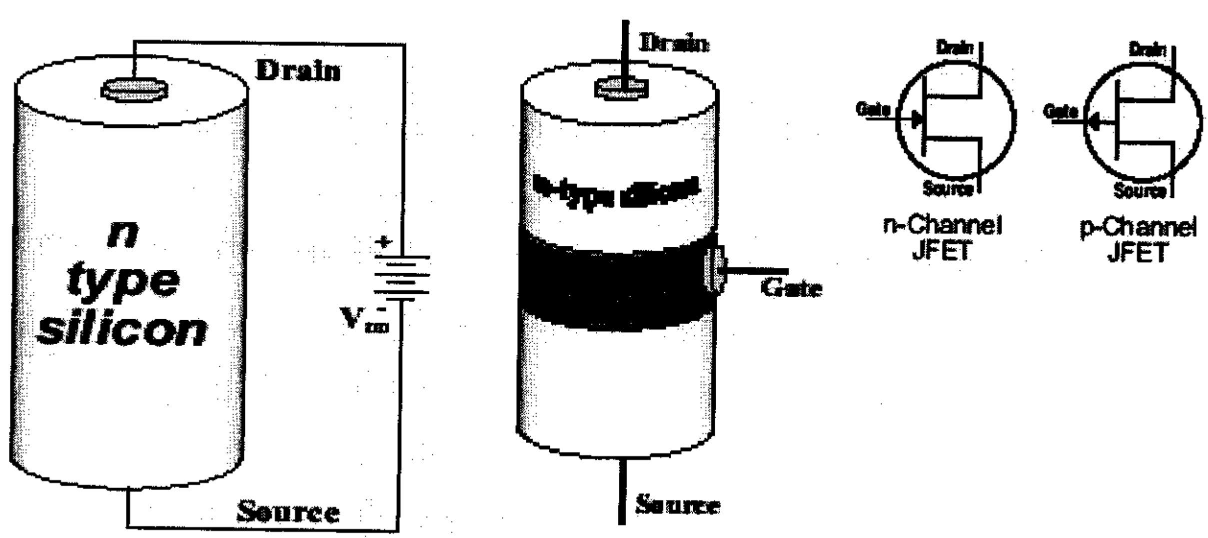
1- The Junction Field Effect Transistor (JFET)

2- The Metal Oxide FET or MOSFET.

6.1 The JFET Constriction

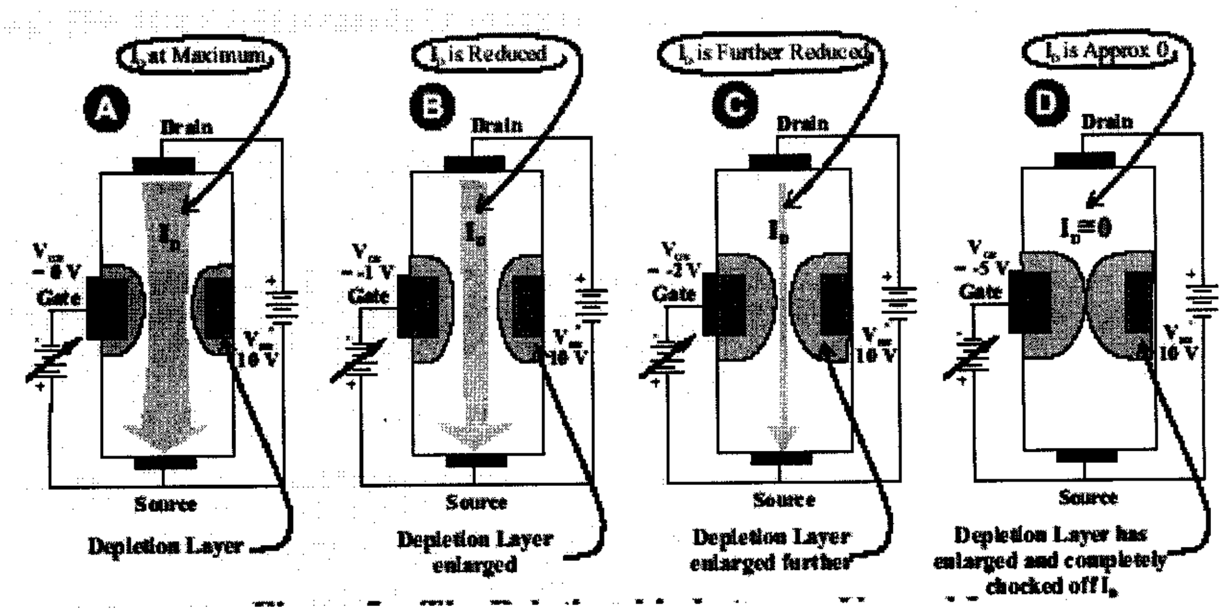
The physical construction of the JFET is significantly different than the BJT. The diagram in Fig(34-a) is the first step in making an n-channel JFET. It is a single piece of n-type silicon semiconductor, with a terminal fused to each end. The lower end is called a & the upper end is called a The supply voltage V forces conventional current to flow from the drain to the source. To complete our JFET, we will add p-type material as shown in Fig. (1-b). It will be in the shape of a collar and surrounds the original n-type silicon. As you can see, there is a channel of n-type material that passes through the collar, hence the name n-channel JFET.

A depletion layer forms in a similar fashion to the PN junction, it has an important function in the operation of the JFET.



6.2 The JFET - Operation Overview

The operation of the JFET is relatively simple. Fig. (2) shows a cross section of the JFET. The voltage source V generates the current through the channel. The voltage source V is used to control this current. By ***varying width of the channel.*** The P-N junction is increased. This reduces the cross sectional area of the conducting n-channel, making it narrower, and thereby increasing the resistance and controlling the drain current I . Increasing V will further constrict the channel and will cause to drop. ***As V increases (becomes more negative) I decreases.***



A- V_{GS} is zero. The maximum drain current I_D is flowing.

B-V_{GS} is increased to -1 V_{GS}. This causes the depletion layer to enlarge into the channel. This reduces the size of the channel, which reduces I_D

C- V_{GS} is increased to -2 V. This causes the depletion layer to enlarge further into the channel which further reduces I_D

D- V_{GS} is increased to -5 V. This causes the depletion layer to enlarge and completely choke off the channel. This causes I_D to be reduced to near zero. The value of V_{GS} that causes I_D to be reduced to this near zero value is called **VGS(off)** .

Control I_D by using V_{DS}

As shown in Fig.() V_{GS} is 0 and V_{DS} is 1. A small depletion layer exists around the gate. The depletion layer exists because of the relationship between V_{GS} and V_{DS}. This means that the P-N junction between the gate and the N-type channel is reverse biased and the depletion layer will grow as wide as necessary to reach equilibrium. This depletion layer extends into the channel and reduces its size.

V_{GS} remains at 0. Note that V_{DS} is now 4 V. This further increases the reverse bias on the gate diode. The depletion layer increases into the channel and reduces the current I_D. At the same time, increasing V_{DS} to 4 V increases the current I_D.

is increasing to reduce the current I. The forces are not yet equal.

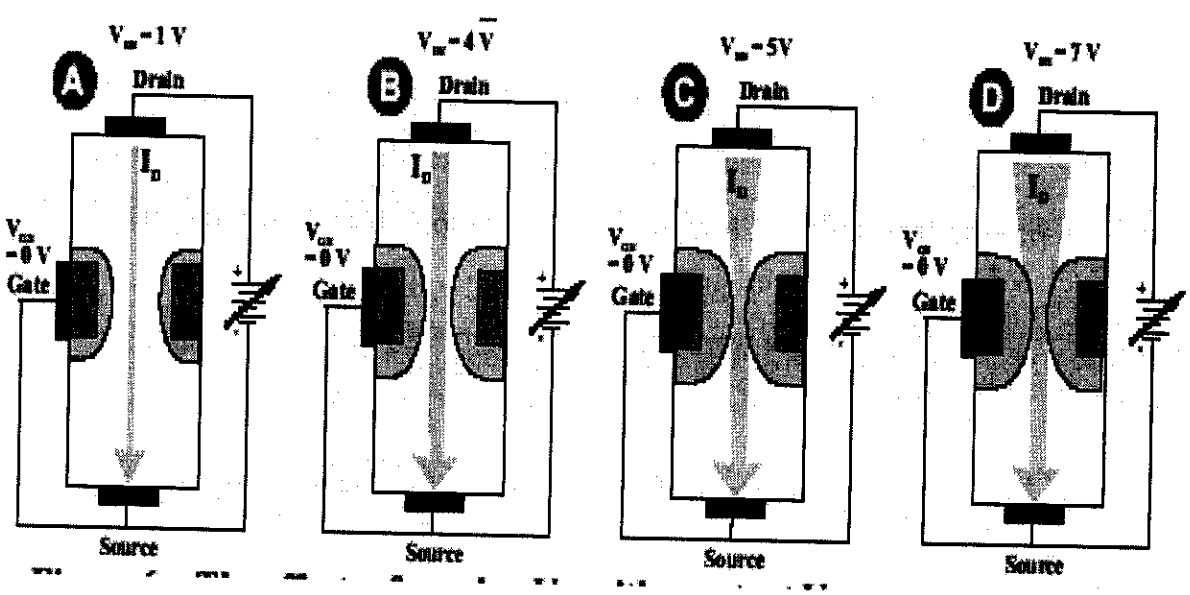
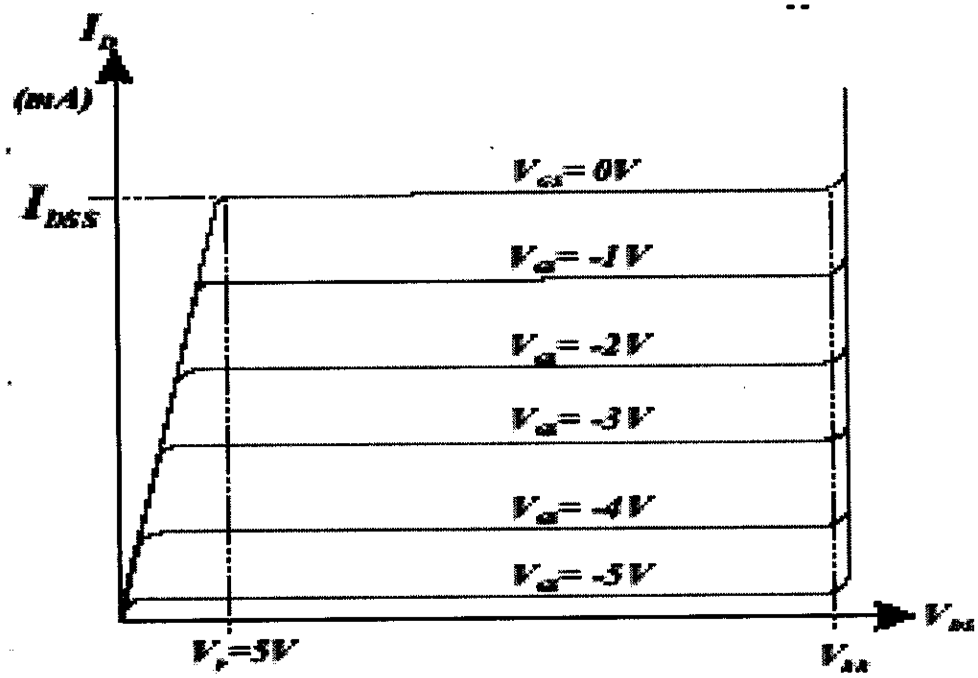


Figure 7 shows the drain curve for the description above. The part of the curve to the left of V_P is called the **Ohmic Region**. As V_{DS} increases from 0 to V_P, the drain current increases. Here, the JFET is acting like a resistor, a linear increase in V_{DS} above V_P, the value of drain current levels off at a relatively constant value ***Constant-Current region.***



The output current (ID) can be defined in terms of the circuit input voltage by

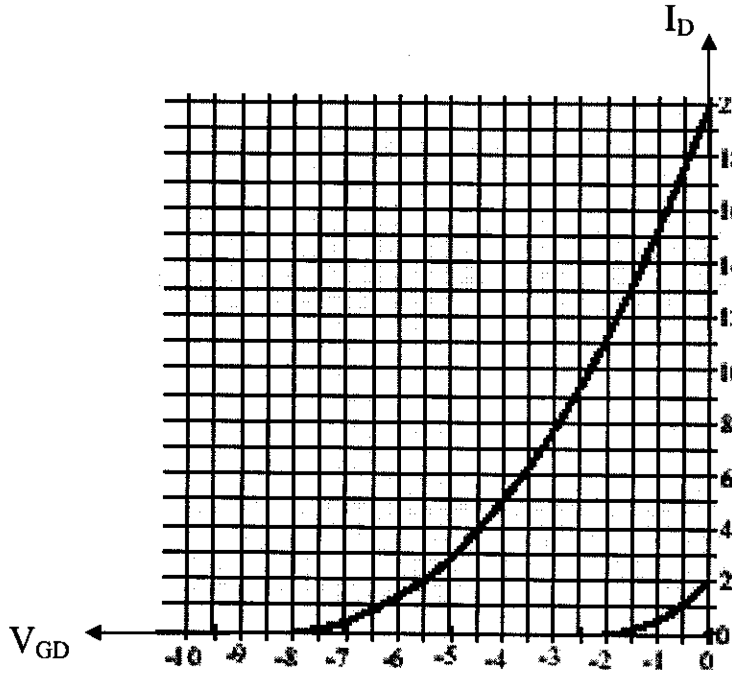
$$I_D = I_{Dss}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

6.3 The Transconductance Curve

Plotting the transconductance curve for a specific JFET is a graph of all possible combinations of V_{GS} and I_D for a specific device. The process for plotting the transconductance curve for a given JFET is as follows:

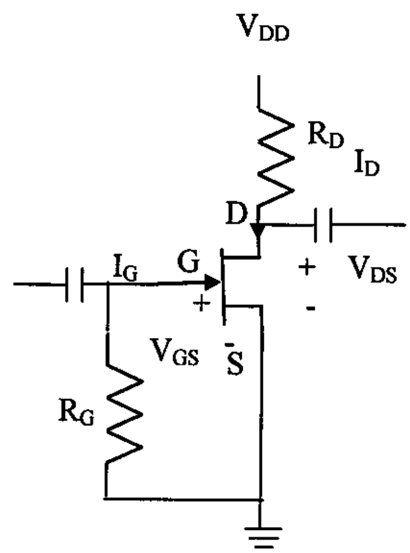
$$g_m = \frac{\partial I_D}{\partial V_{Gs}}$$

$$g_m = \frac{2\ I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$



5.4 DC Bias of JFET

The C.S cct. shown below, the analysis of this cct. is



- The C.S without V_{GG} and R_S

  - input loop

$-I_G R_G - V_{GS} = 0$

$I_G = 0$ (R.B)

$V_{GS} = 0$ volt

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

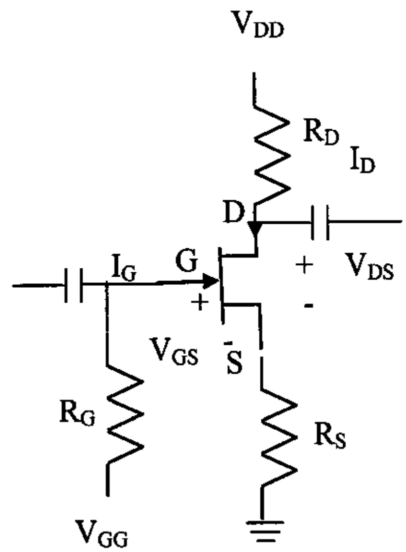
  - output loop

$$V_{DD} - I_D R_D - V_{DS} = 0$$
$$V_{DS} = V_{DD} - I_D R_D$$

Q (V_{DS}, I_D)

- The C.S with V_{GG}, R_S, or both

  - input loop



$V_{GG} - I_G R_G - V_{GS} - I_S R_S = 0$

$I_G = 0$ (R.B)

$I_S = I_D$

$V_{GS} = V_{GG} - I_S R_S$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GG} - I_D R_S}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GG} - I_D R_S}{V_P} + \left(\frac{V_{GG} - I_D R_S}{V_P}\right)^2\right)$$

$$I_{DSS}\left(\frac{R_S}{V_P}\right)^2 I_D^2 + \left(\left(\frac{2 I_{DSS} R_S}{V_P}\right) - \left(\frac{2 I_{DSS} V_{GG} R_S}{V_P}\right) - 1\right) I_D$$

$$+\left(I_{DSS} - 2 I_{DSS}\left(\frac{V_{GG} R_S}{V_P^2}\right) + I_{DSS}\left(\frac{V_{GG}}{V_P}\right)^2\right) = 0$$

$$A I_D^2 + B I_D + C = 0$$

This equtION Solve by

$$I_{D1,2} = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}$$

  - output loop

$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$

$V_{DS} = V_{DD} - I_D (R_D + R_S)$

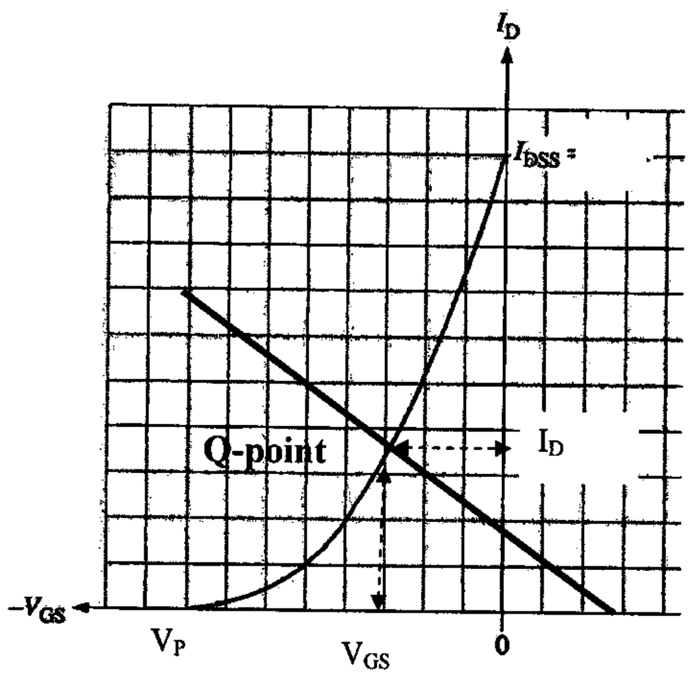
Q (V_{DS}, I_D)

2- Graphical methods

By draw eqs. (1) and (2) the crossing point is the solution as shown below

I_D	V_{GS}
I_{DSS}	0
$I_{DSS}/2$	$V_p/4$
$I_{DSS}/4$	$0.3\ V_P$
0	V_P

I_D	V_{GS}
0	V_{GG}
I_{DSS}	$V_P - R_S / I_{DSS}$



(I_D, V_{GS})

- output loop

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$$
$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Q (V_{DS}, I_D)

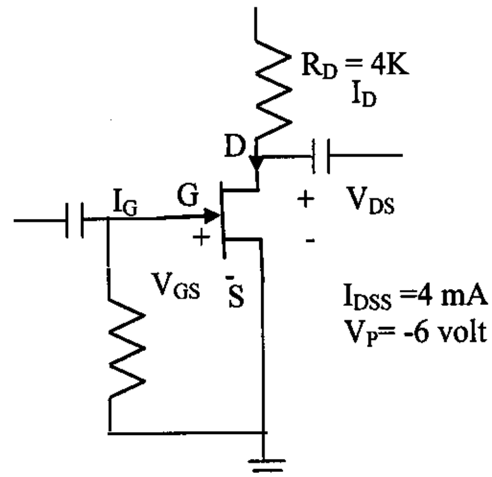
Example/ For the cct. shown below find V_{GS}, I_D, V_{DS}, and g_m

SOL/

- input loop

$I_G R_G - V_{GS} = 0$

$I_G = 0$ (R.B)



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 4 * 10^{-3}\left(1 - \frac{0}{-6}\right)^2 = 4 \quad mA$$

$V_{GS} = 0$ volt

- output loop

$$V_{DD} - I_D R_D - V_{DS} = 0$$
$$V_{DS} = V_{DD} - I_D R_D$$
$$V_{DS} = 10 - 4 * 10^{-3} * 1 * 10^3$$
$$V_{DS} = 6 \ volt$$

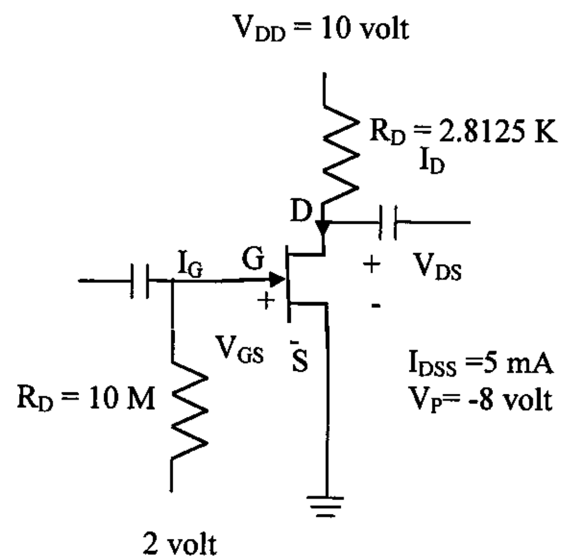
Q ($V_{DS} = 6$ volt, $I_D = 4$ mA)

$$g_m = \frac{2\ I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_m = \frac{2\ 4 * 10^{-3}}{6}\left(1 - \frac{0}{-6}\right) = 1.33\ m\ \frac{1}{\Omega}$$

Example/ For the cct. shown below find V_{GS}, I_D, and V_{DS}

SOL/



- input loop

$V_{GG} - I_G R_G - V_{GS} = 0$

$I_G = 0$ (R.B)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 5 * 10^{-3}\left(1 - \frac{-2}{-8}\right)^2$$

$$I_D = 2.8125 \quad mA$$

$V_{GS} = -2$ volt

- output Loop

$$V_{DD} - I_D R_D - V_{DS} = 0$$
$$V_{DS} = V_{DD} - I_D R_D$$
$$V_{DS} = 10 - 2.8125 * 10^{-3} * 0.9 * 10^3$$
$$V_{DS} = 7.468 \ volt$$

Q (V_{DS} = 7.468 volt, I_D = 2.8125 mA)

Example/ For the cct. shown below find V_{GS}, I_D, V_{DS}, and g_m

SOL/

- input loop

$-I_G R_G - V_{GS} - I_D R_S = 0$

$I_G = 0$ (R.B)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 12 * 10^{-3}\left(1 - \frac{V_{GS}}{-6}\right)^2$$

V_{GS} = -680 I_D volt

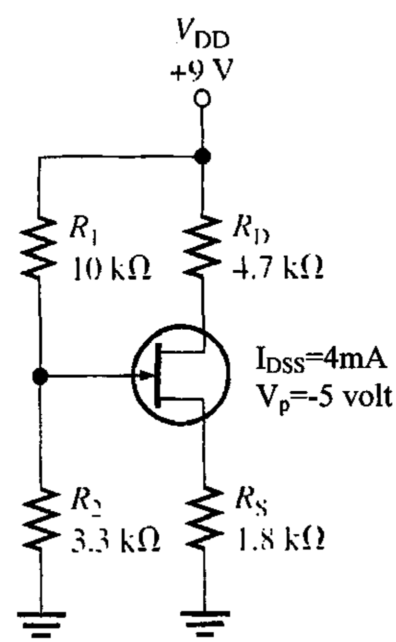
By use mathematical or graphical solution the I_D and V_{GS} are

I_D= 3.8 mA V_{GS}= -2.6 V

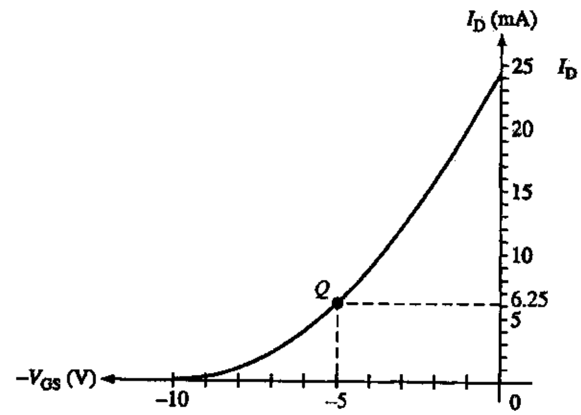
$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$
$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$
$$V_{DS} = 12 - 3.8 * 10^{-3} * 2.18 * 10^3$$
$$V_{DS} = 3.72 \; volt$$

SHEET

Q1/ For the cct. shown below find V_{GS}, I_D, V_{SD}, and g_m



Q2) Determin the value of R_S and R_D required to self bias N- channel JFET cct. that has the transfer characteristic curve shown below. V_{DS} = 5 volt V_{DD} =15 volt.



Q3/ For the cct. shown below find V_{GS}, I_D, V_{GD}, V_{DS}